

FIG. 1

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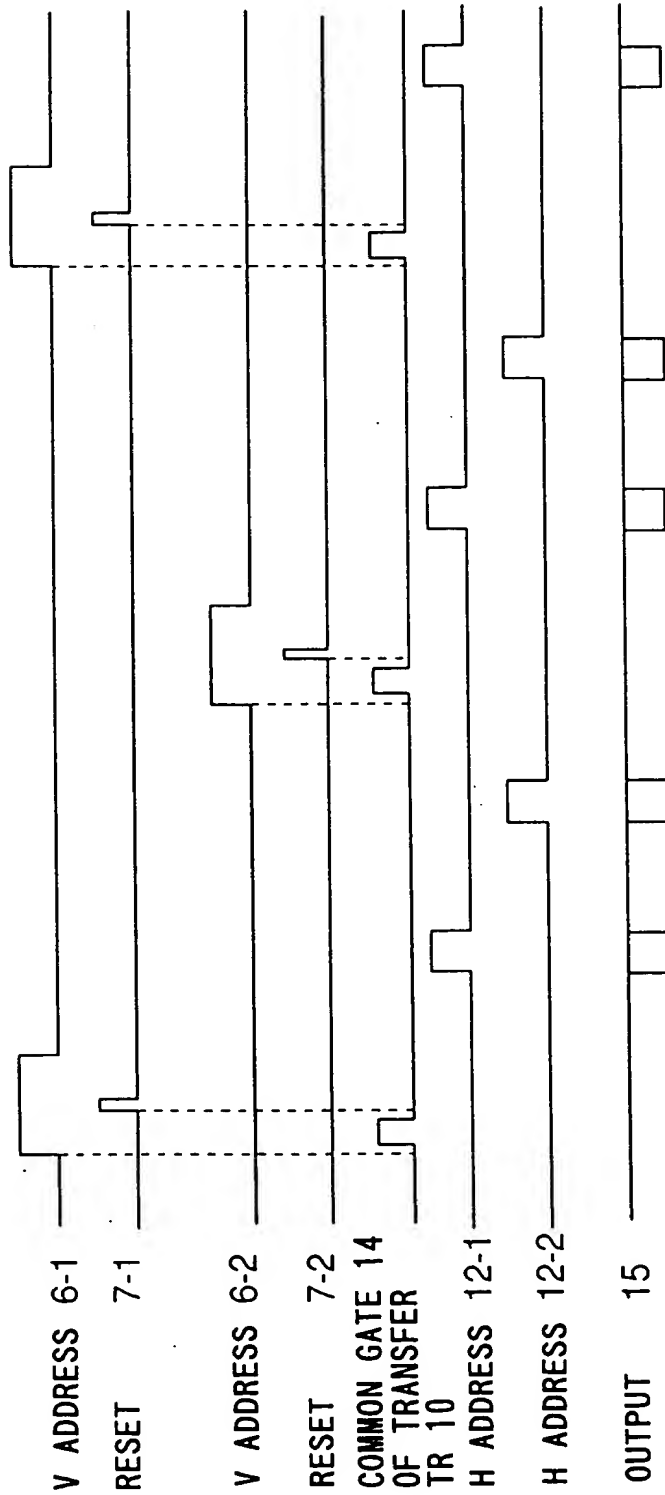


FIG. 2

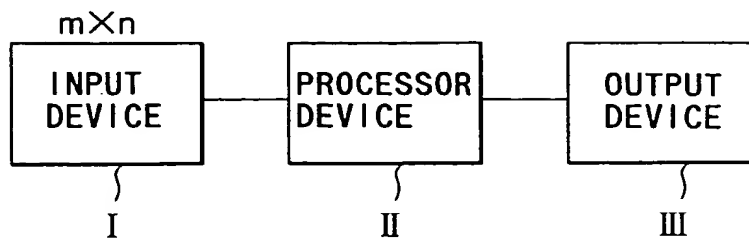


FIG.3

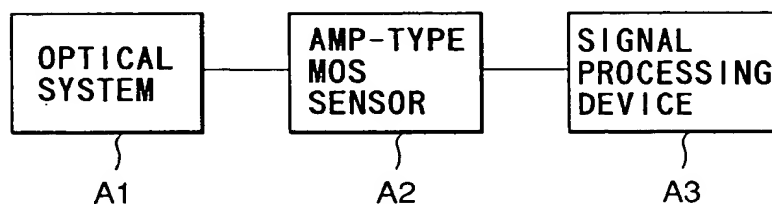


FIG.4

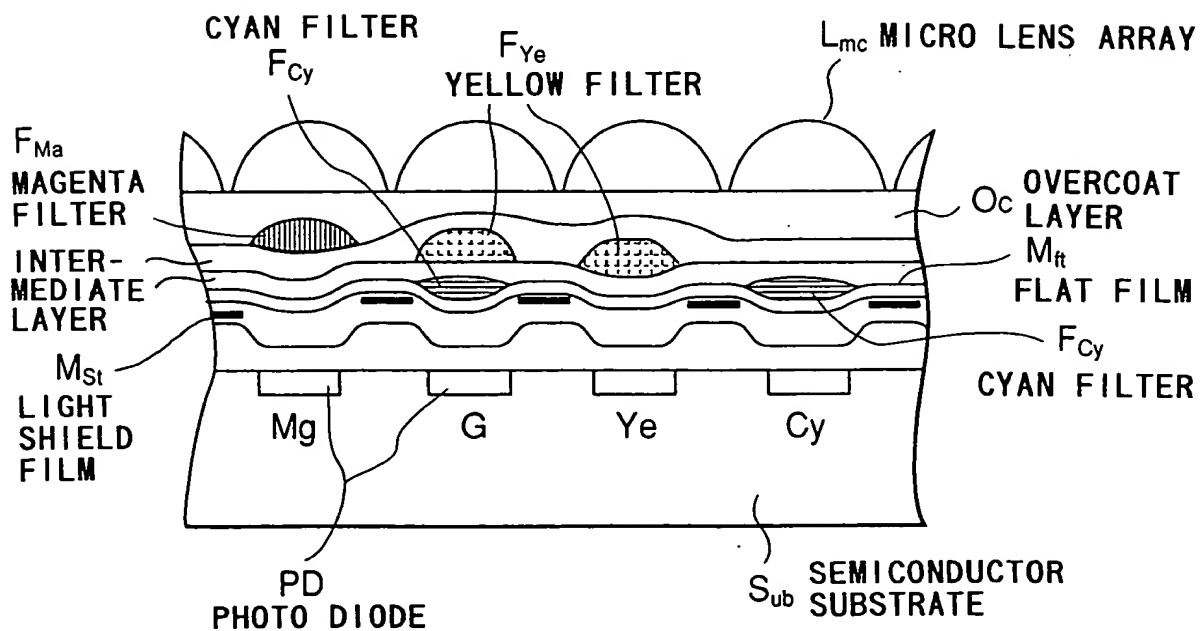


FIG.6

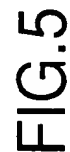


FIG. 5

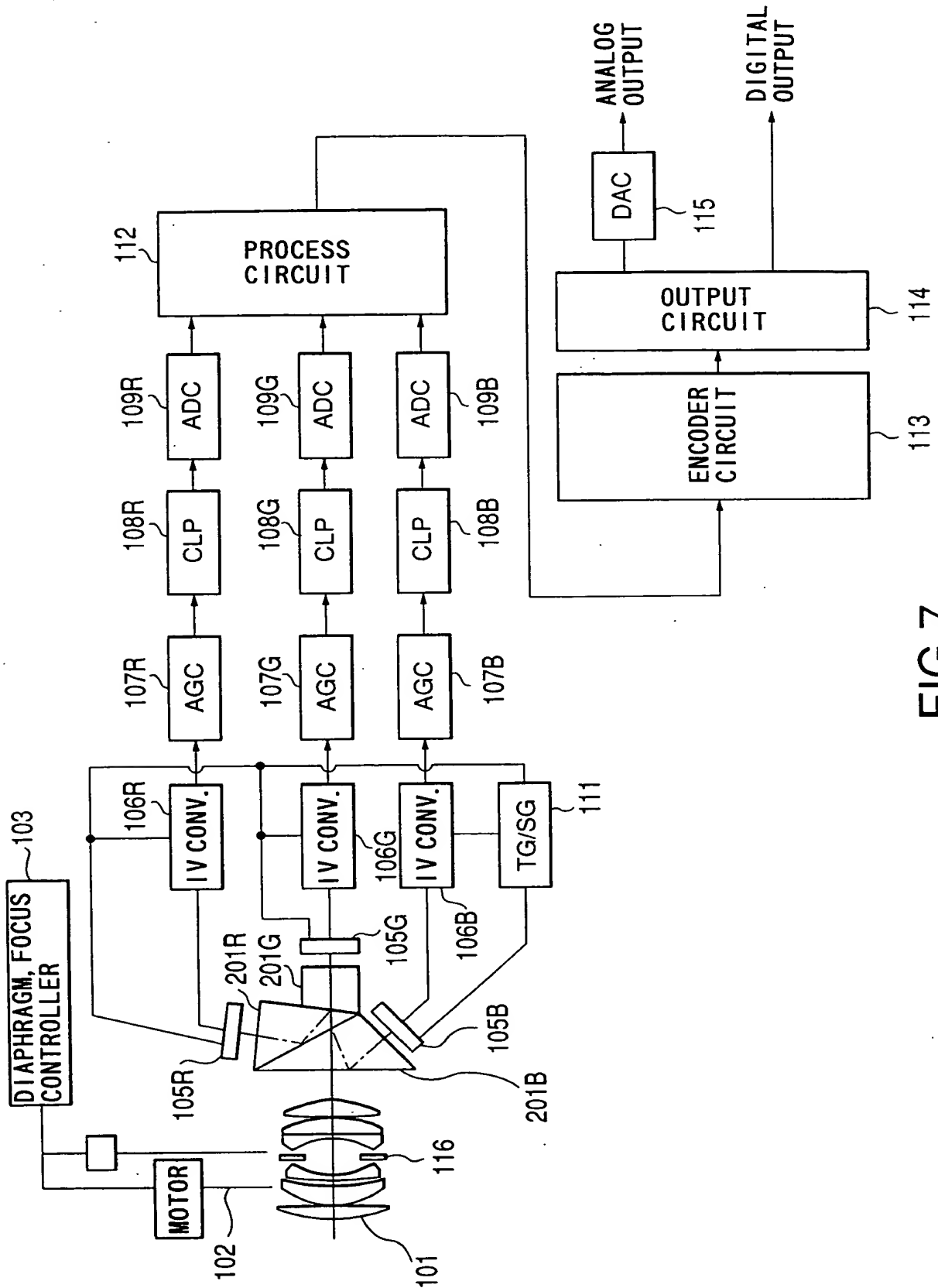


FIG.7

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100, 100-2

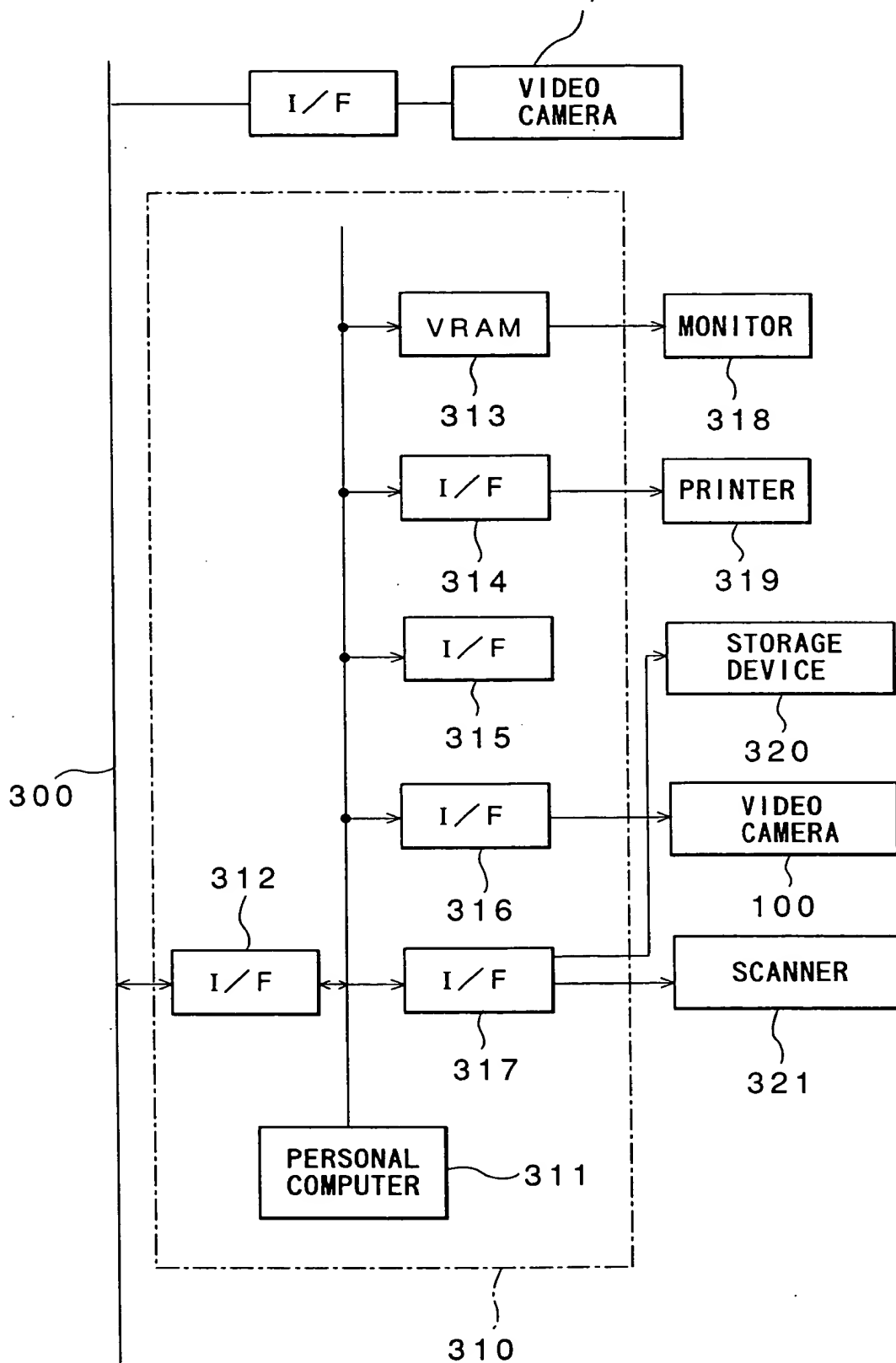


FIG. 8

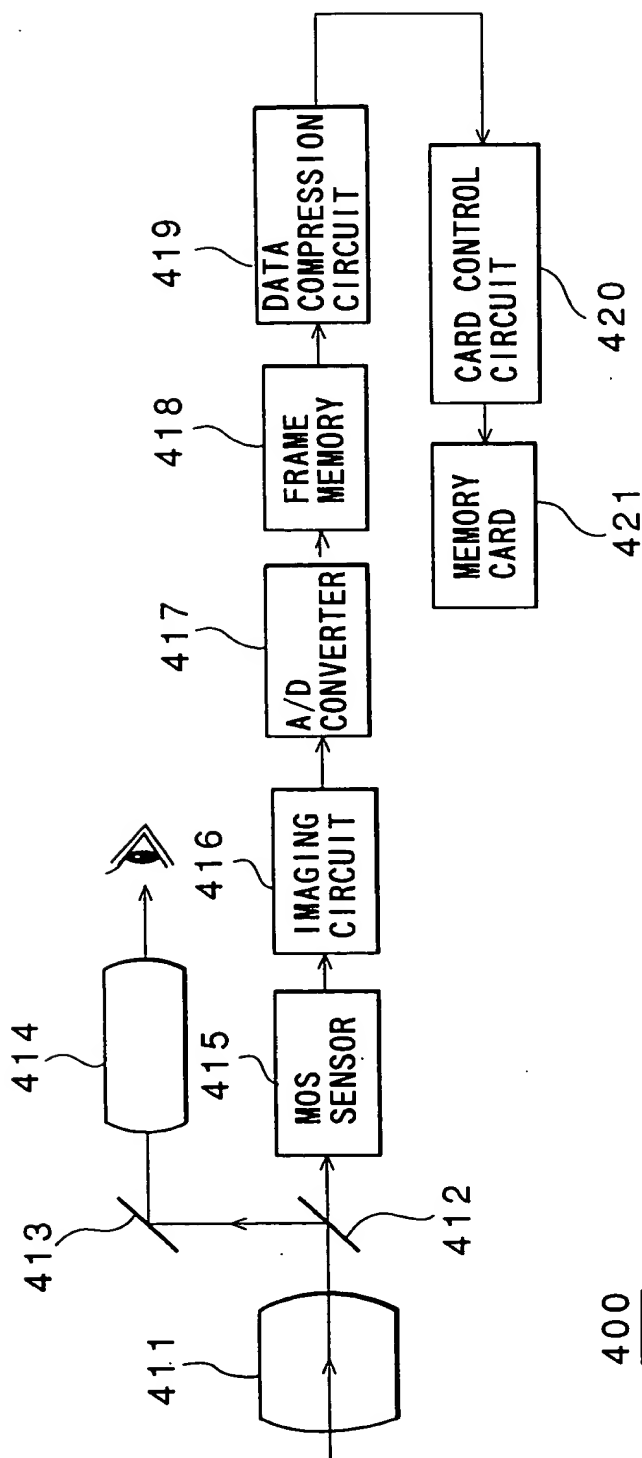


FIG. 9

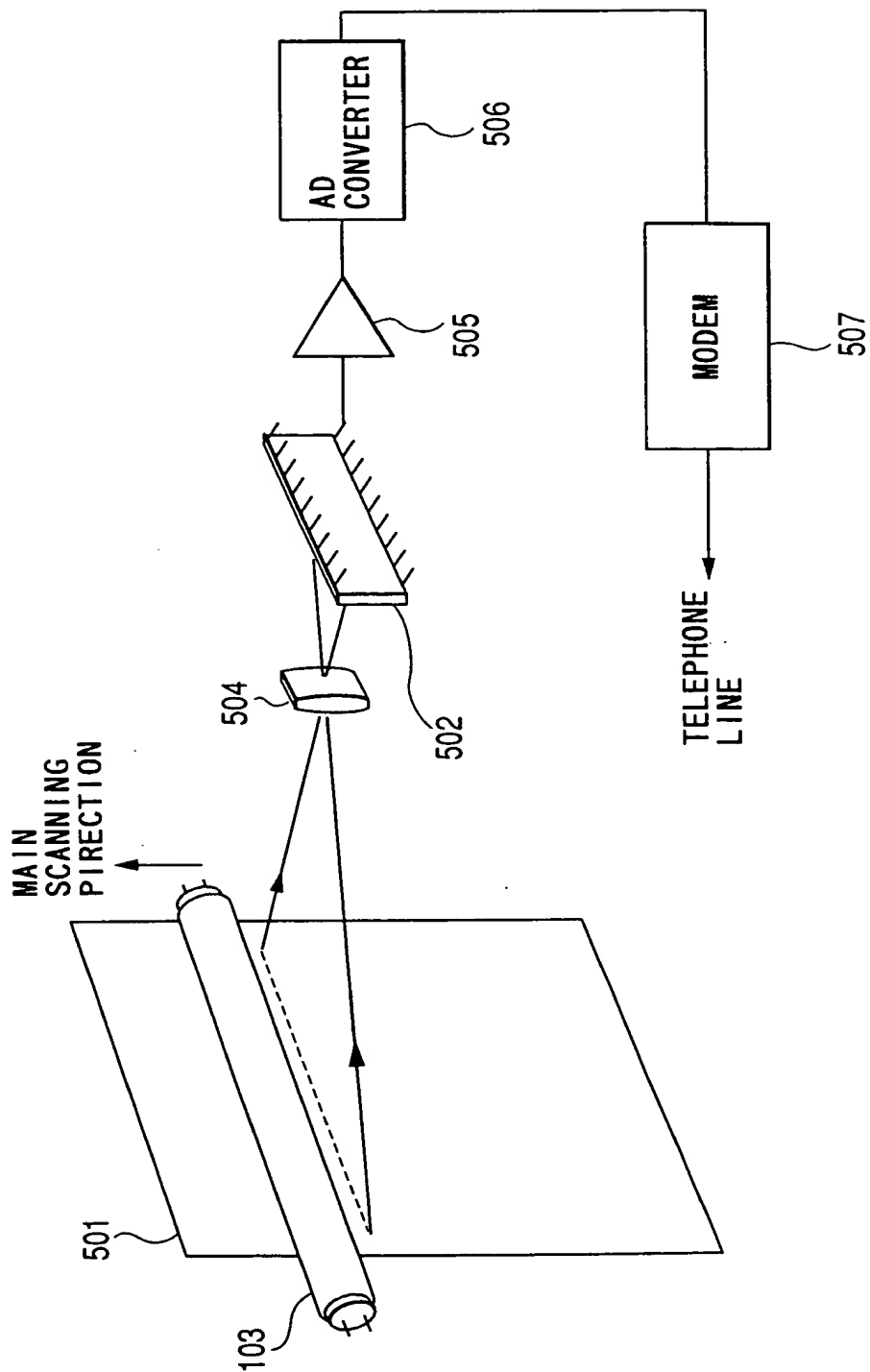


FIG.10

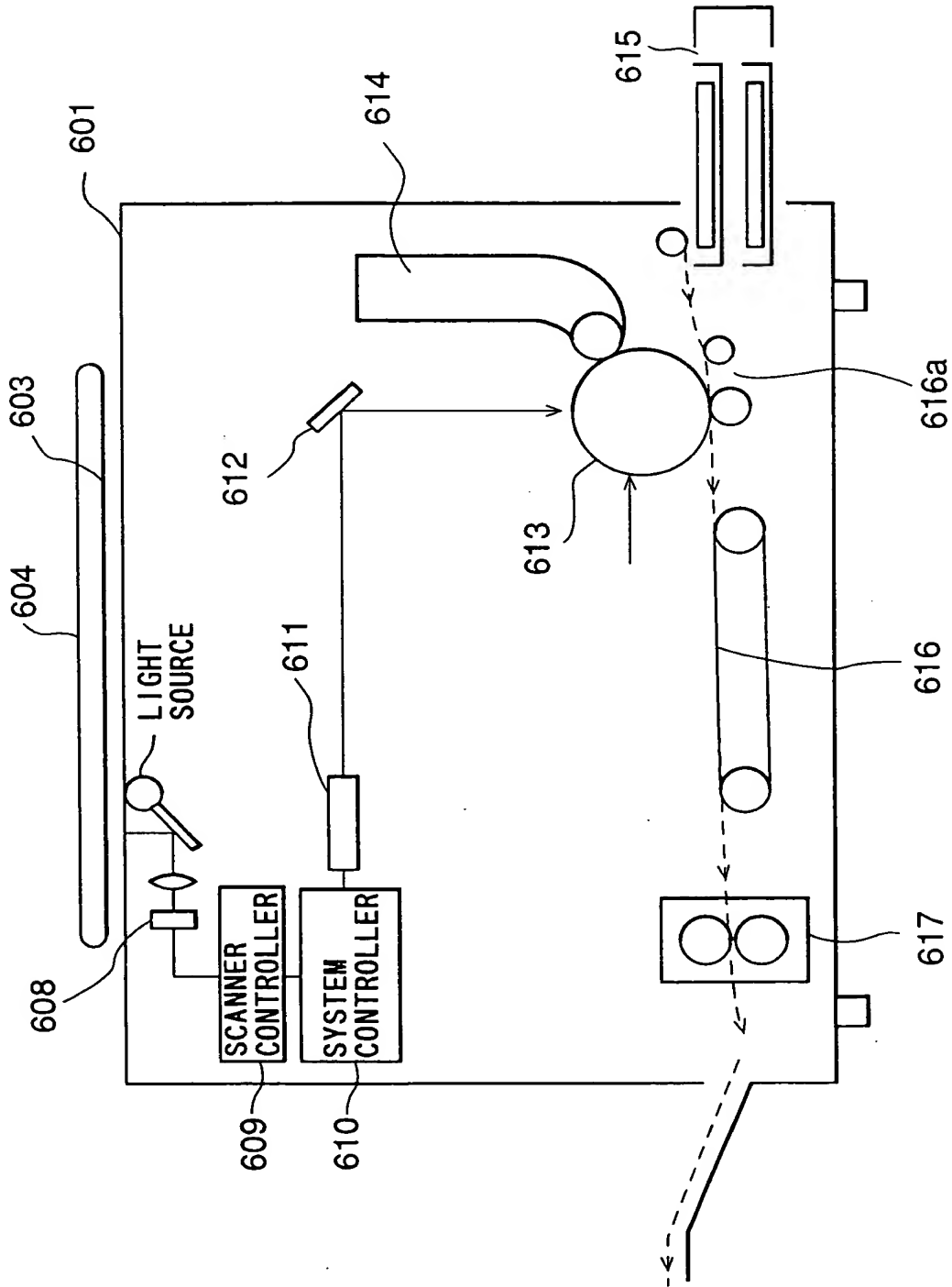


FIG.11

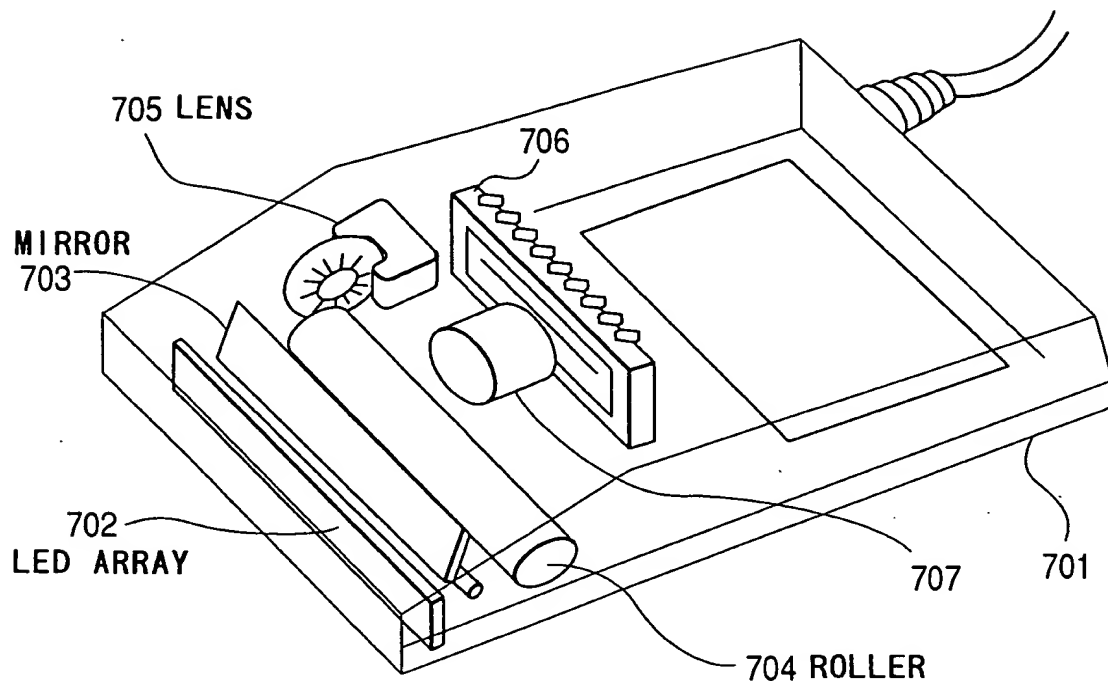


FIG.12

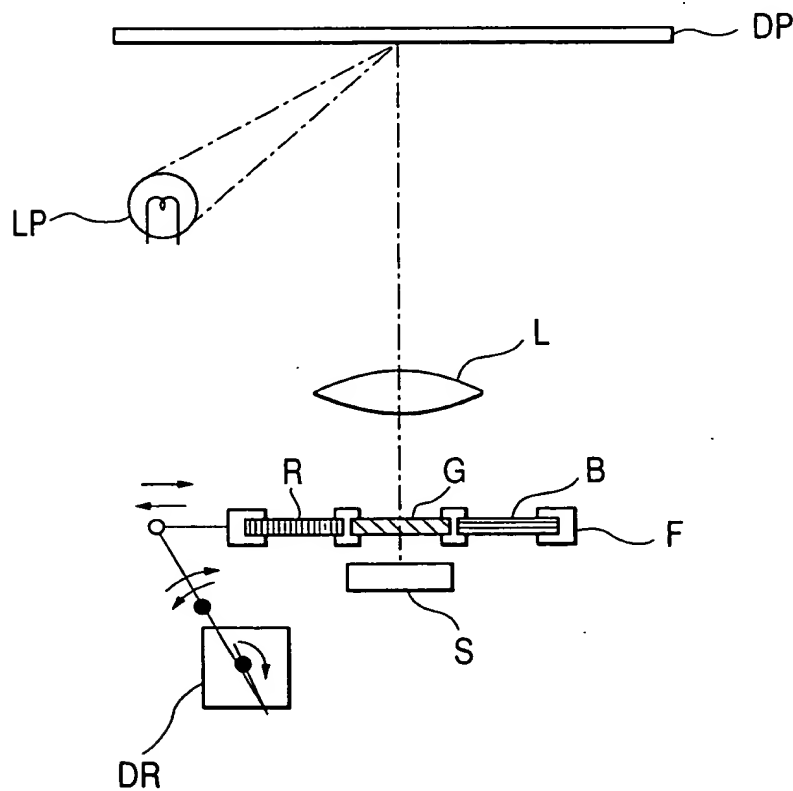


FIG.13

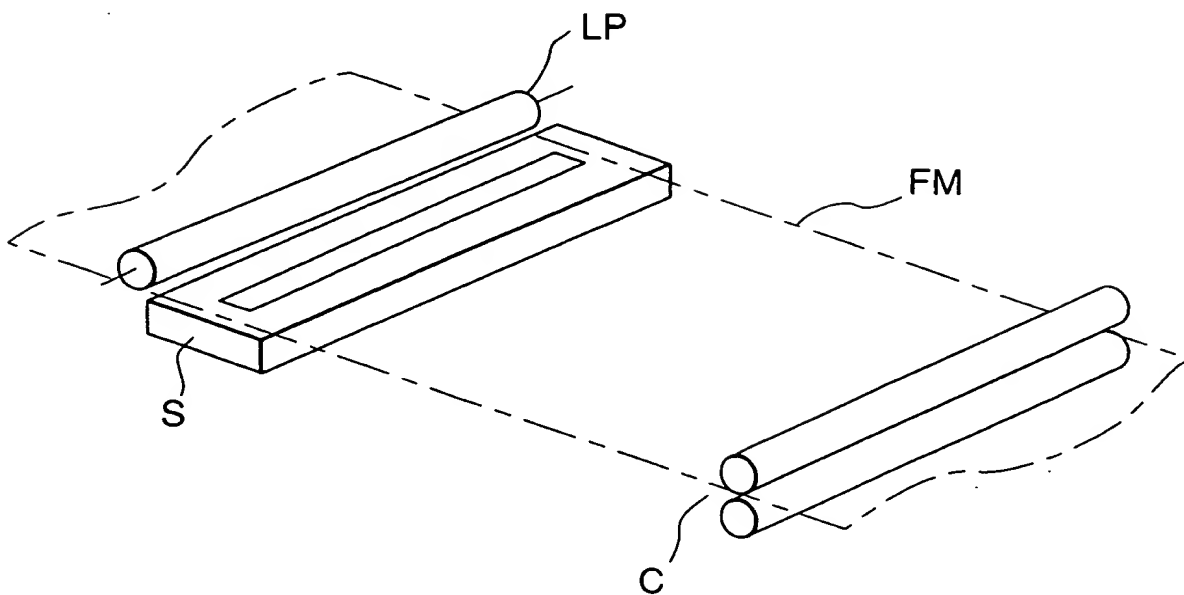


FIG. 14

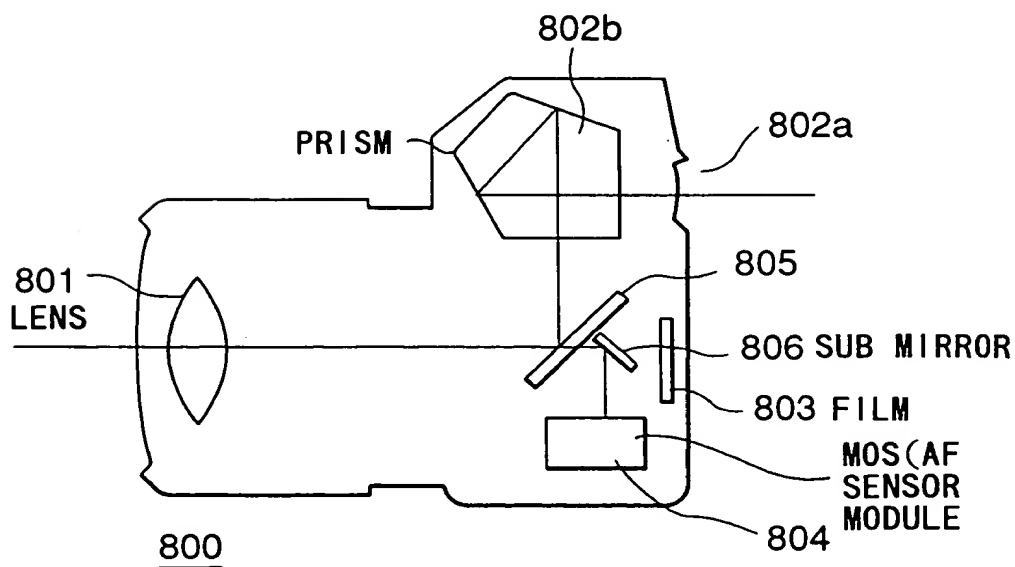
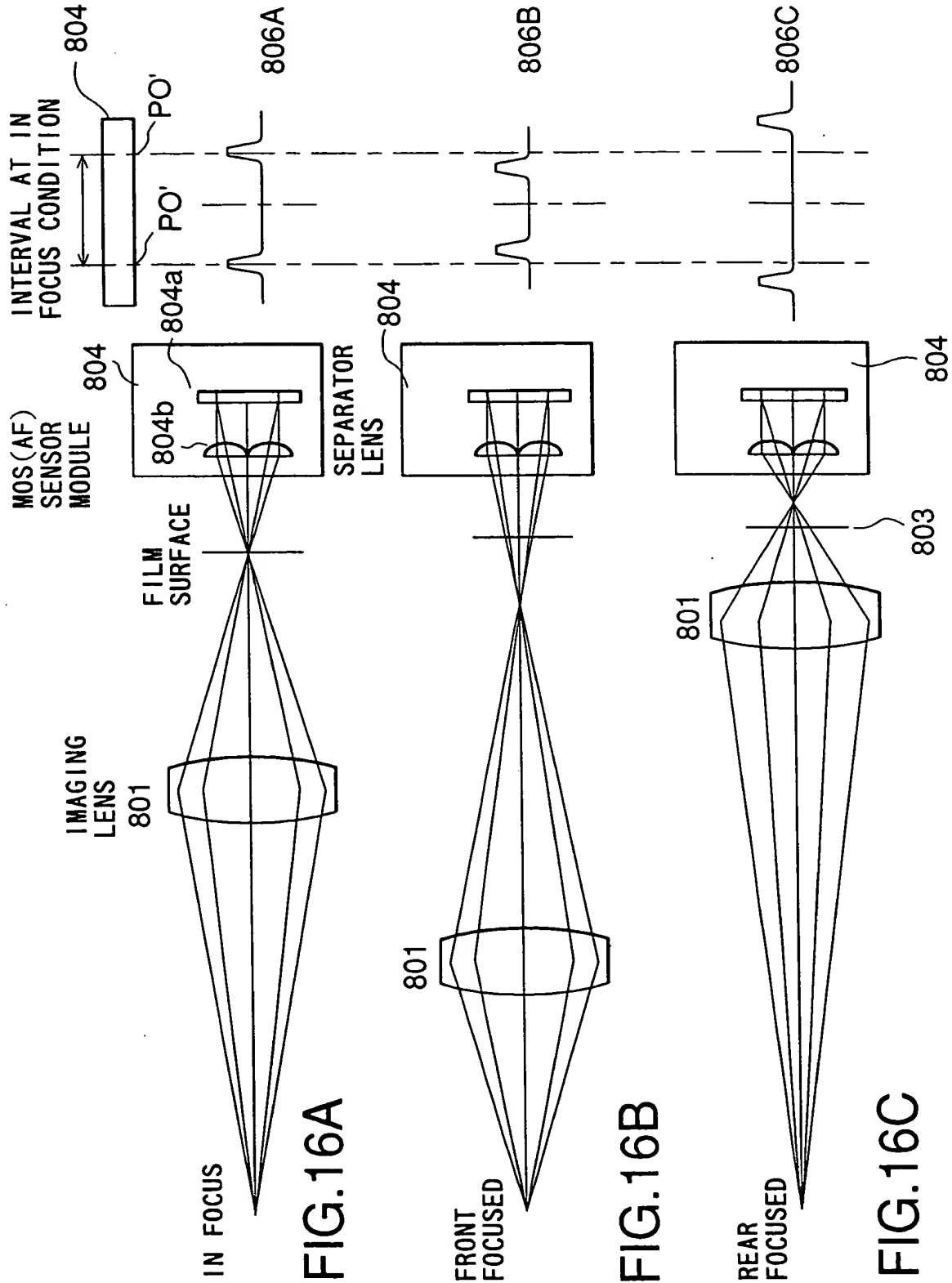


FIG. 15





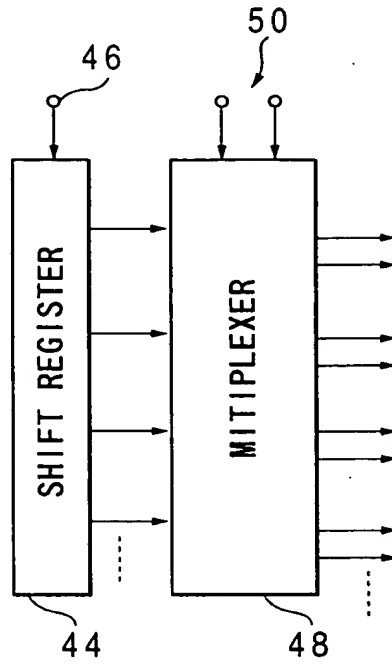


FIG.18

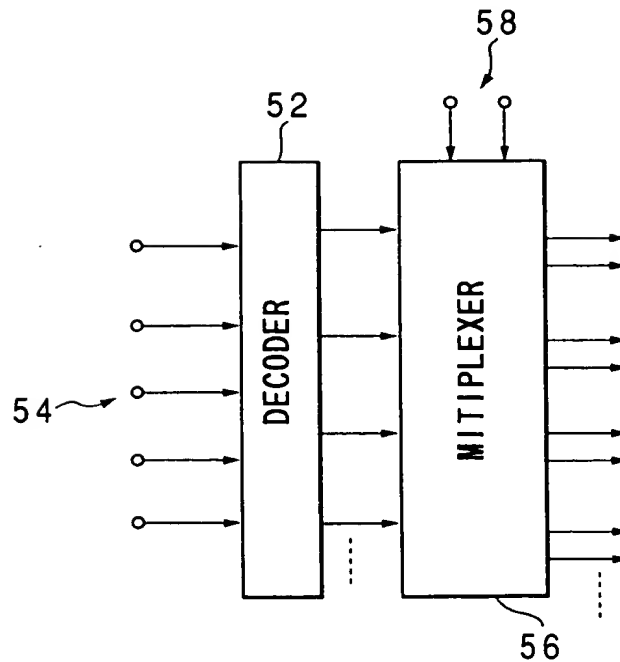


FIG.19

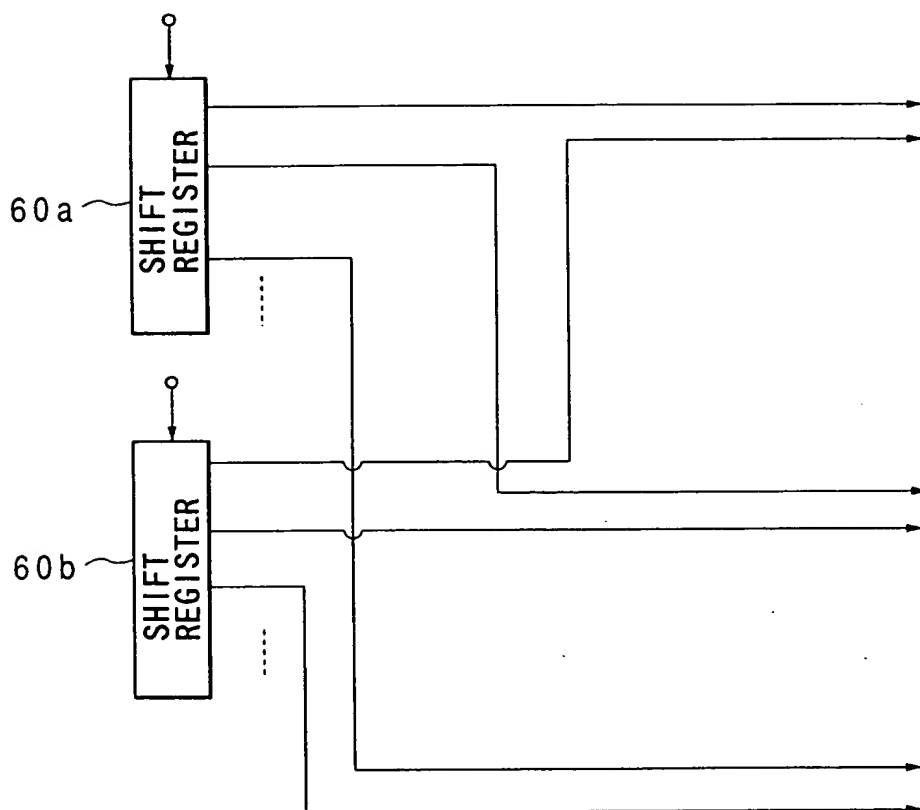


FIG.20

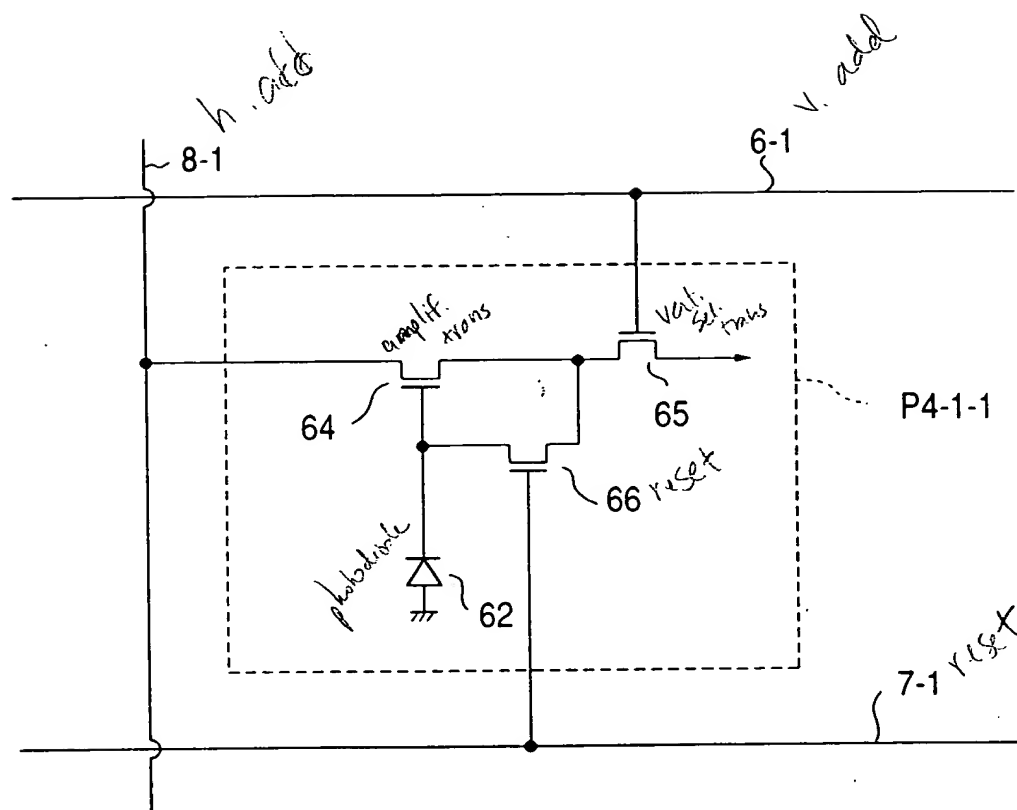


FIG.21

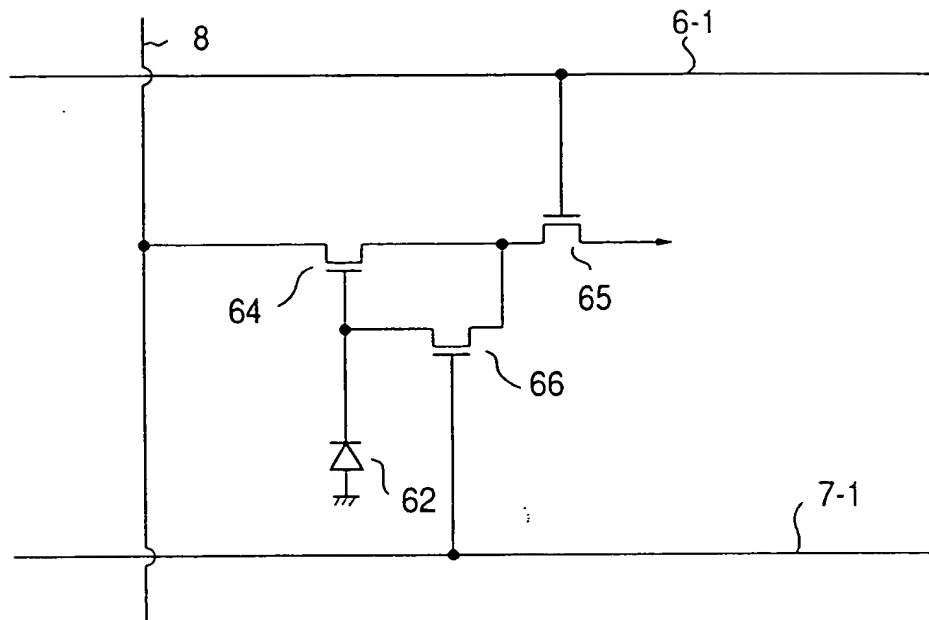


FIG.22A

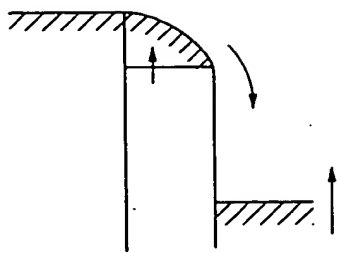


FIG.22B

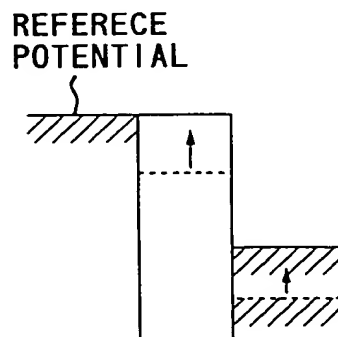


FIG.22C

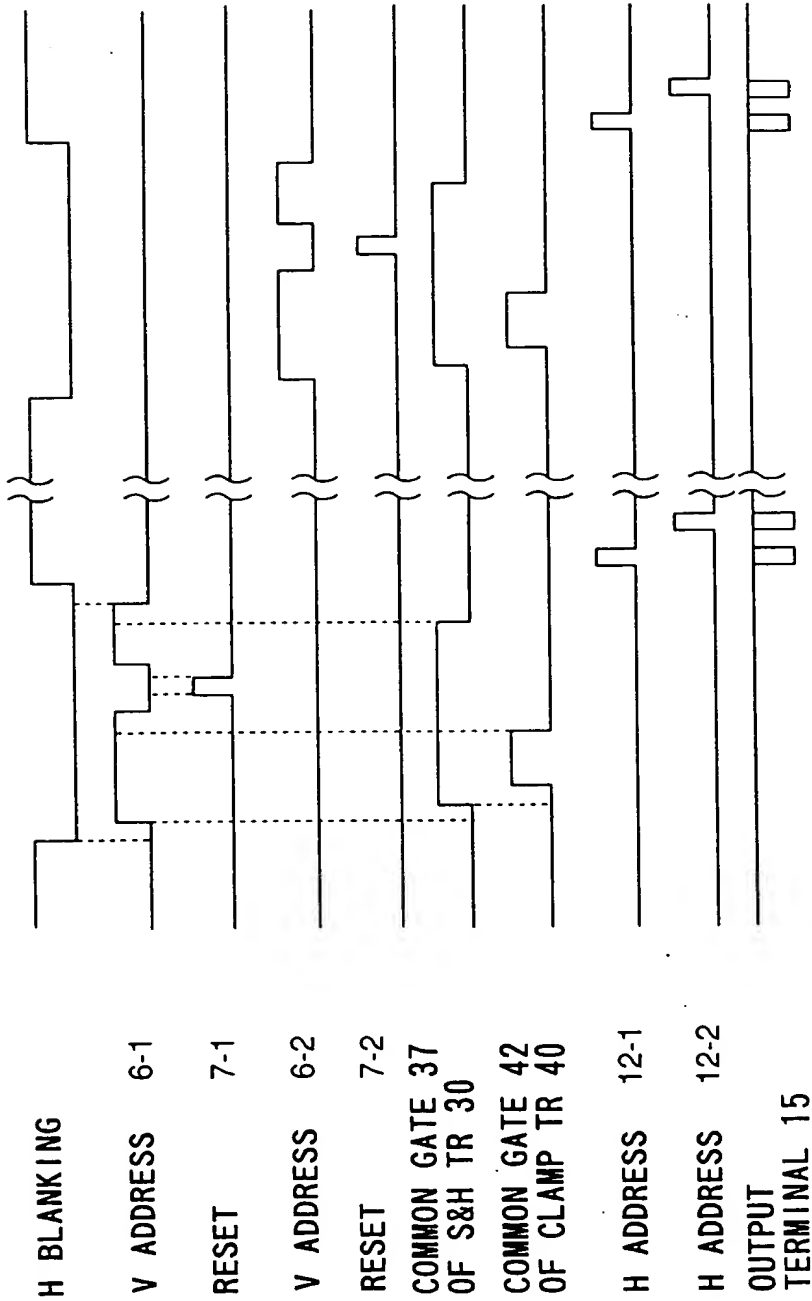


FIG.23

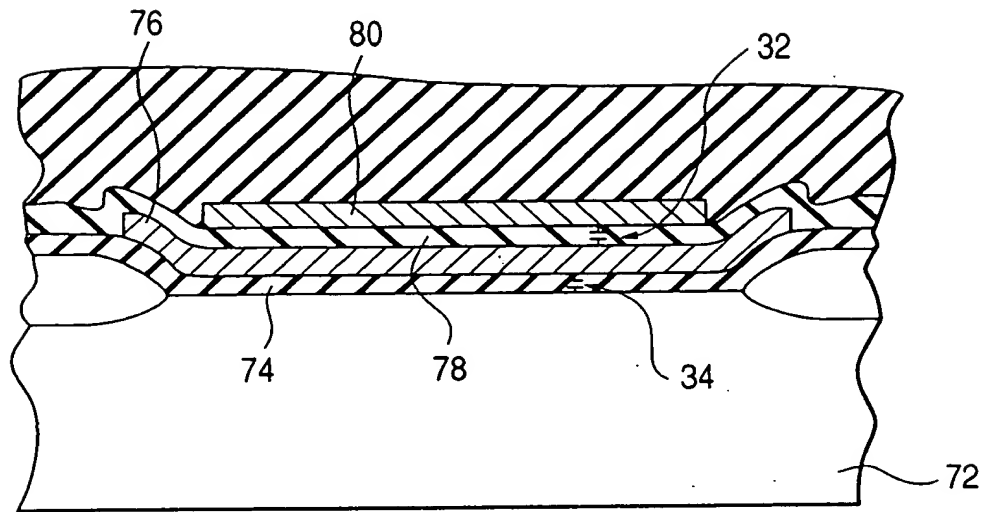


FIG.24

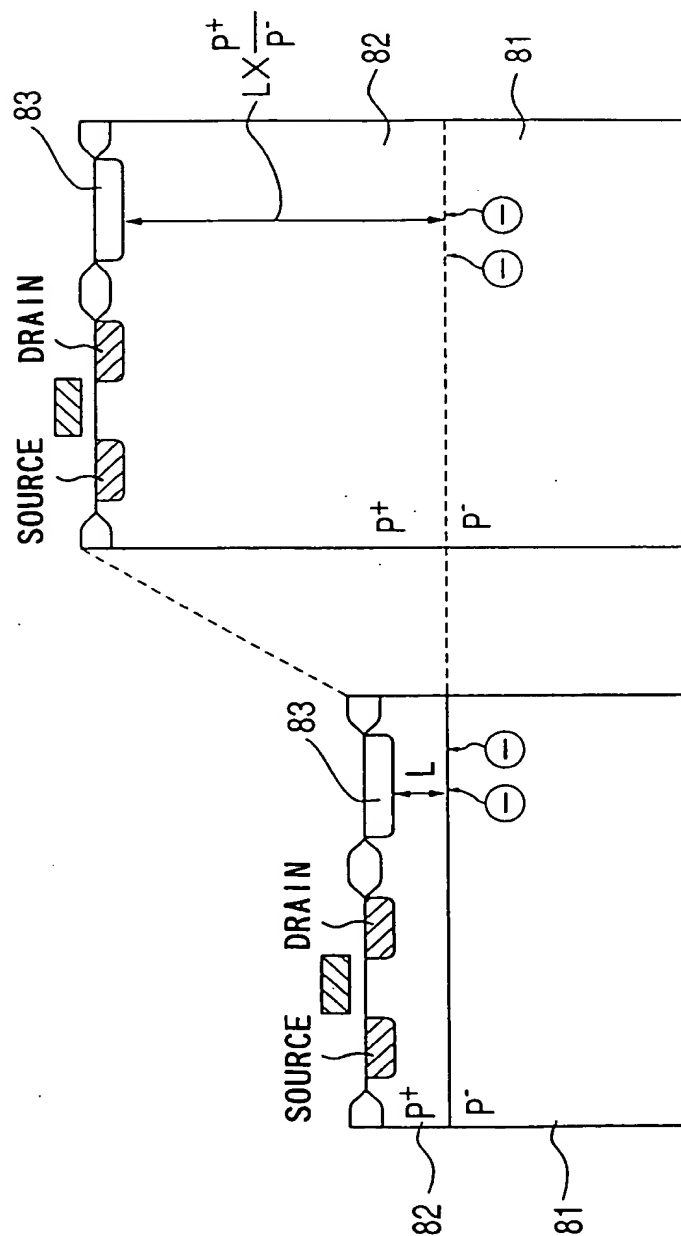


FIG.25B

FIG.25A

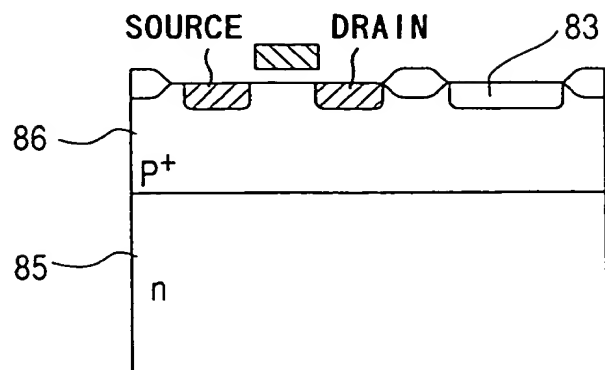


FIG.26

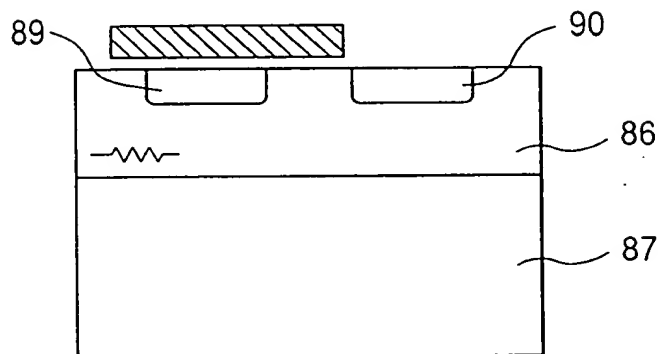


FIG.27

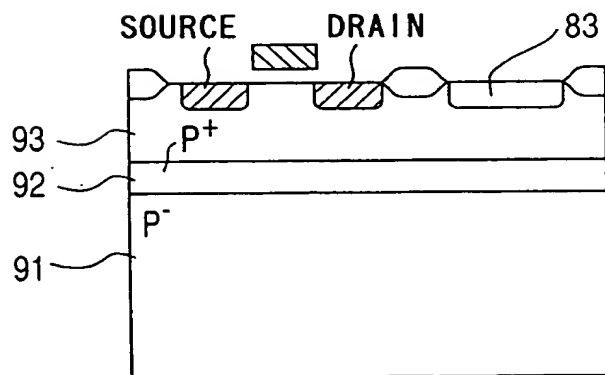


FIG.28

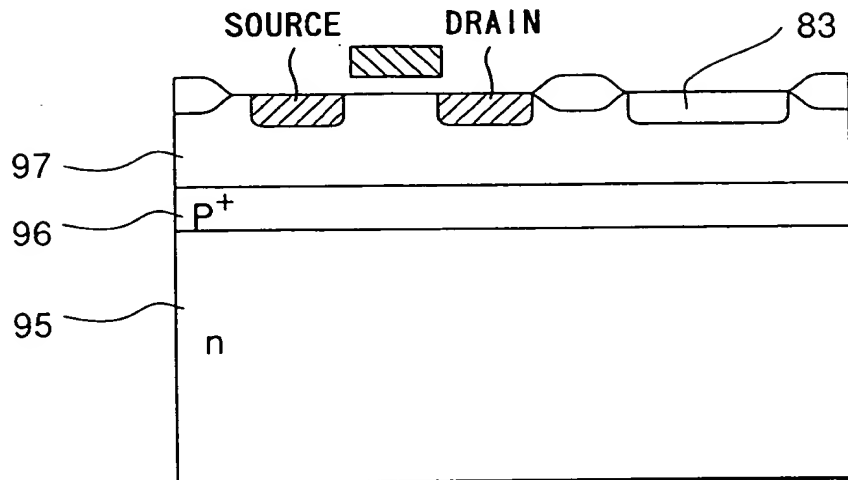


FIG.29

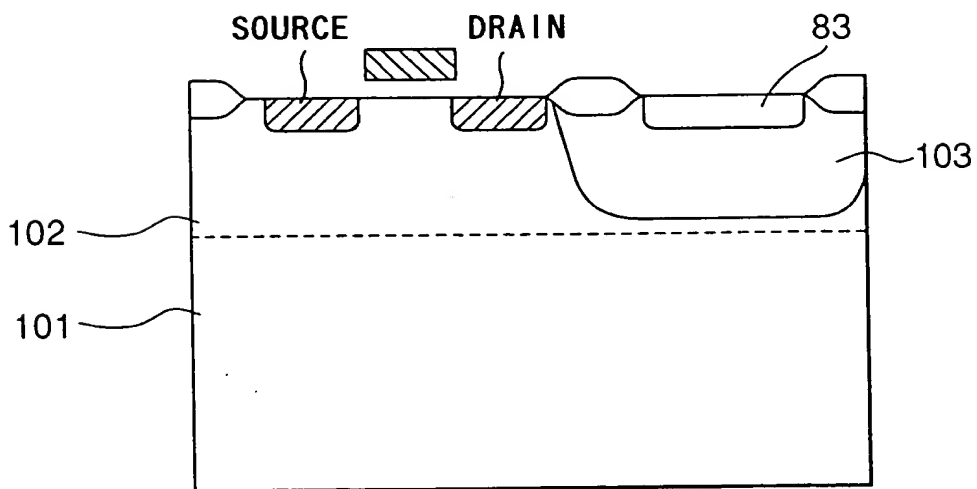


FIG.30

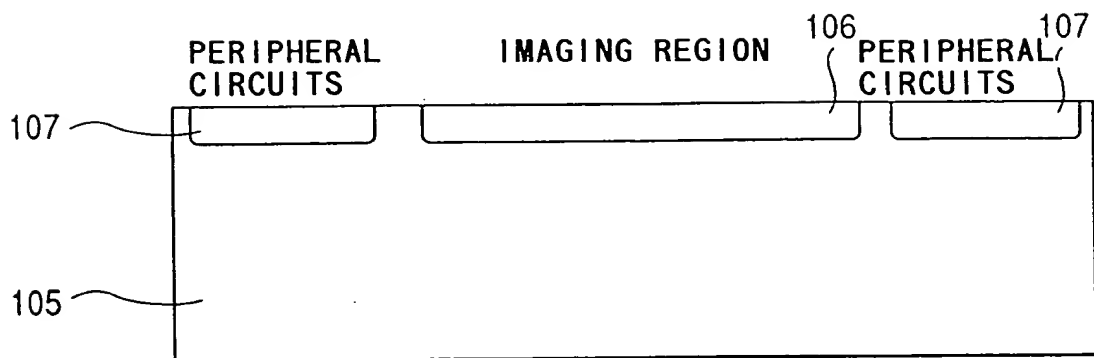


FIG. 31

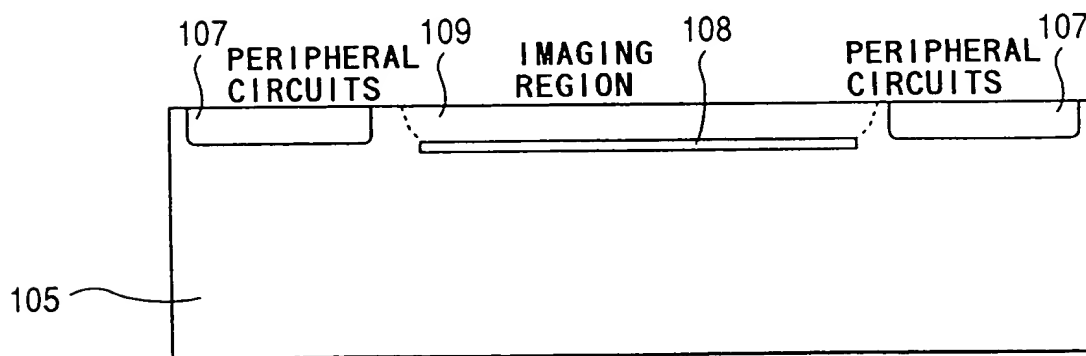


FIG. 32

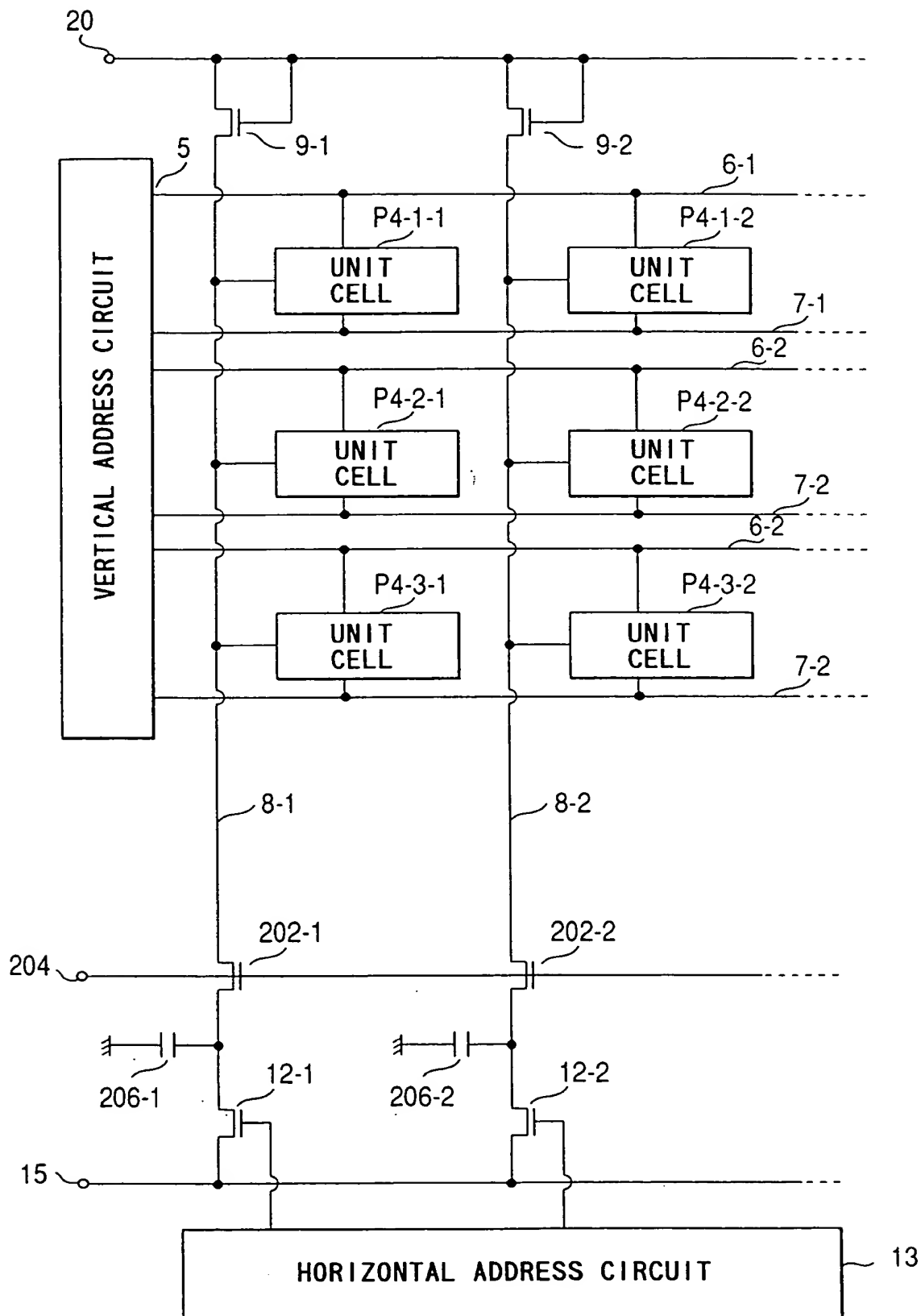


FIG.33

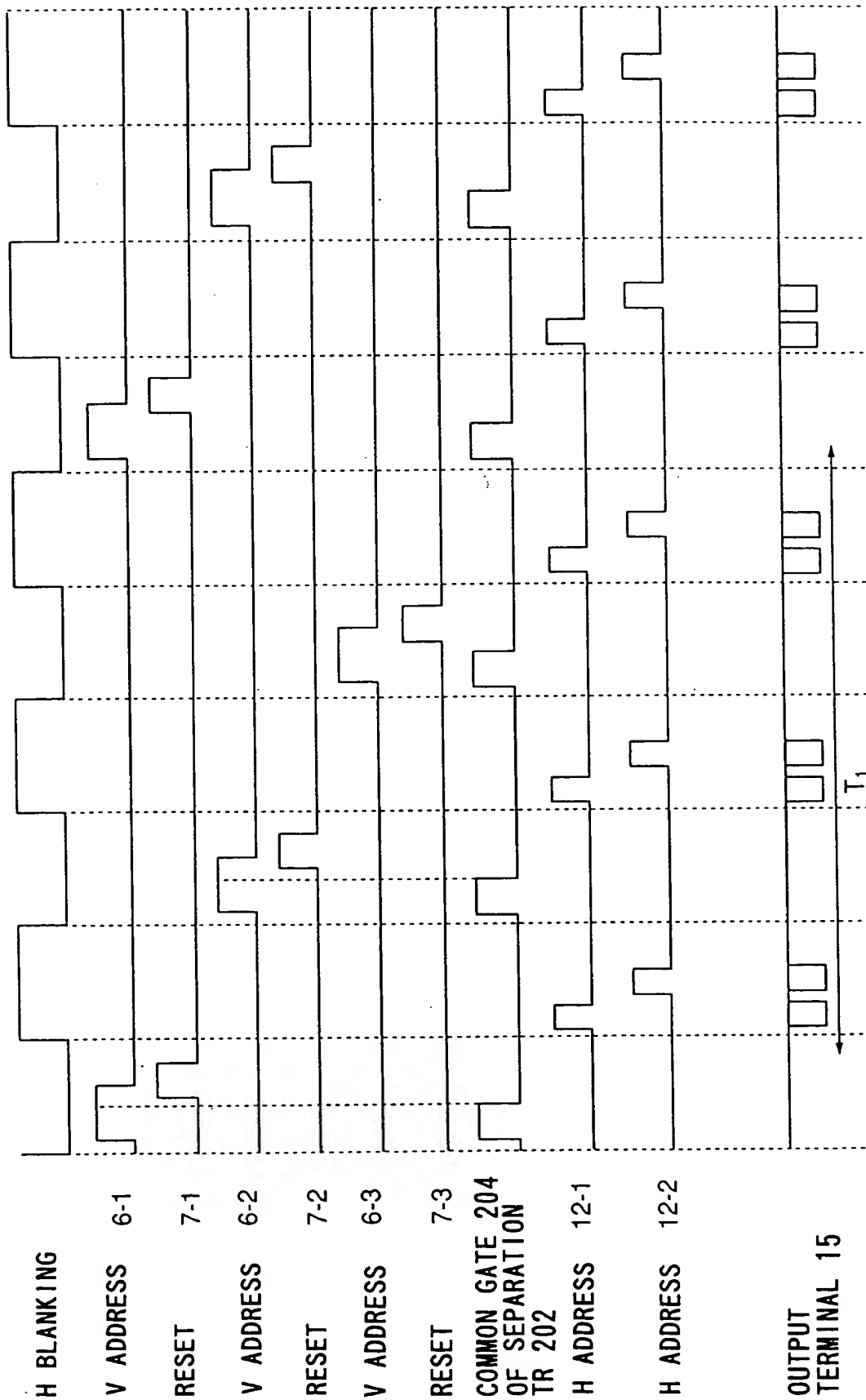


FIG.34

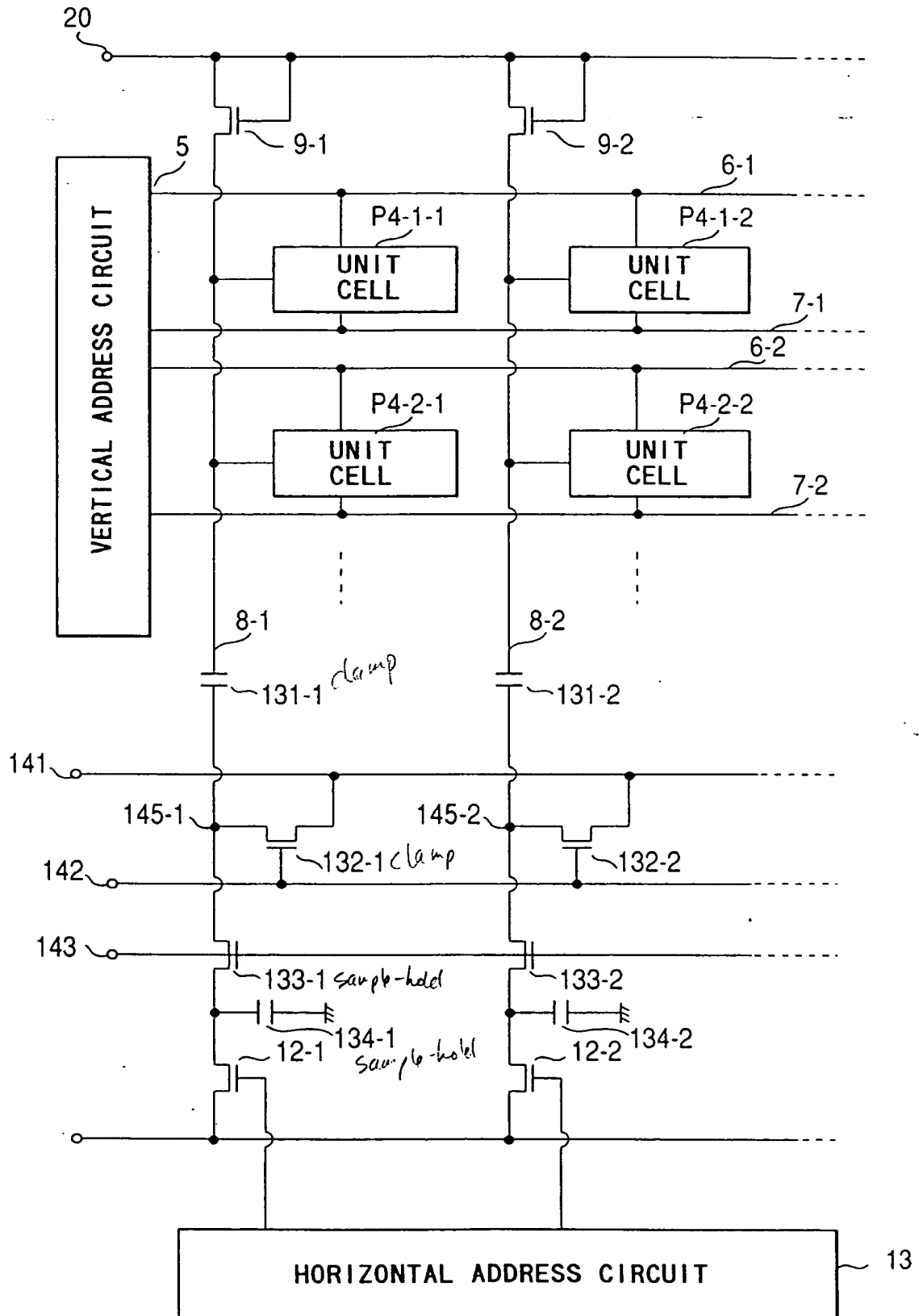


FIG.35

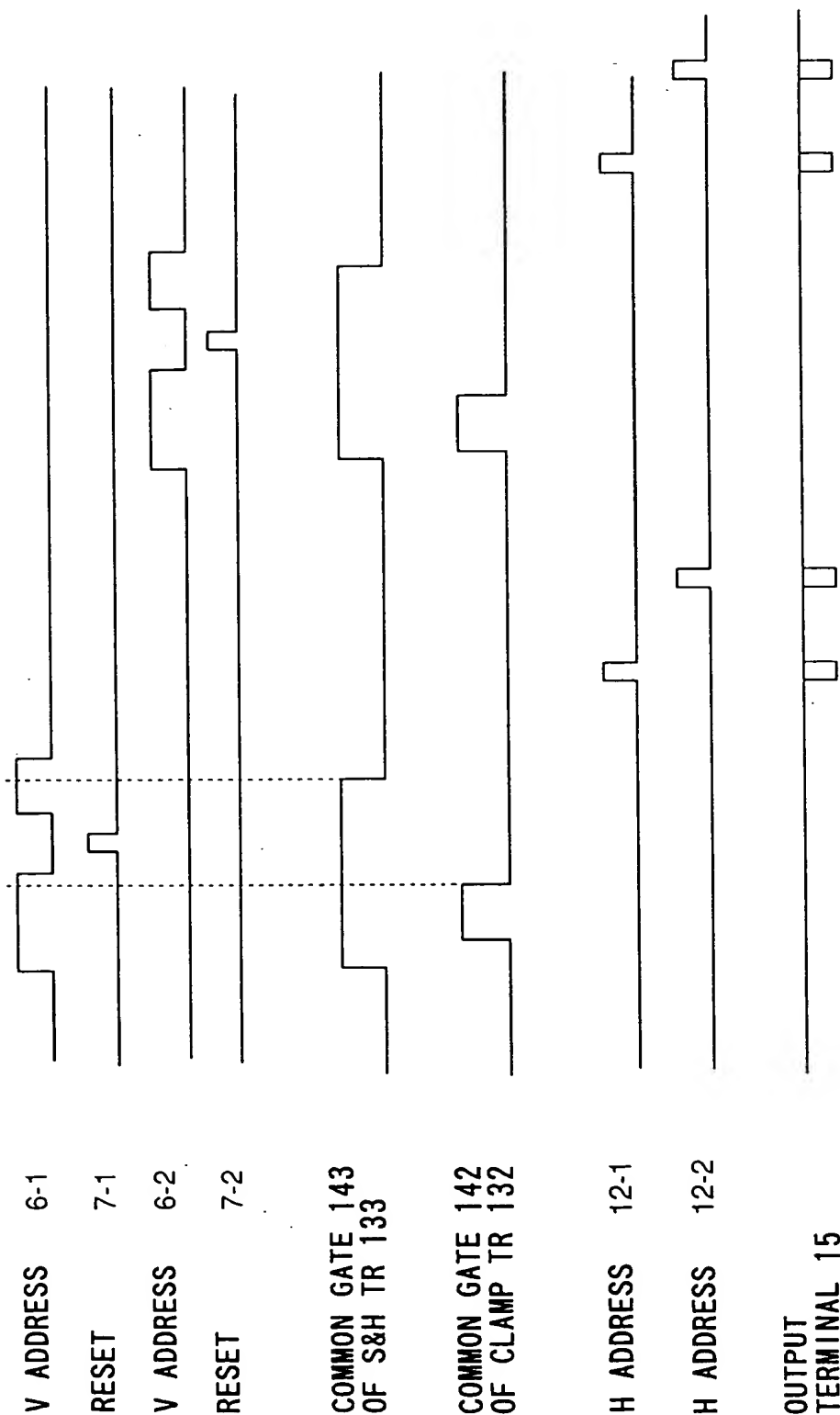


FIG.36

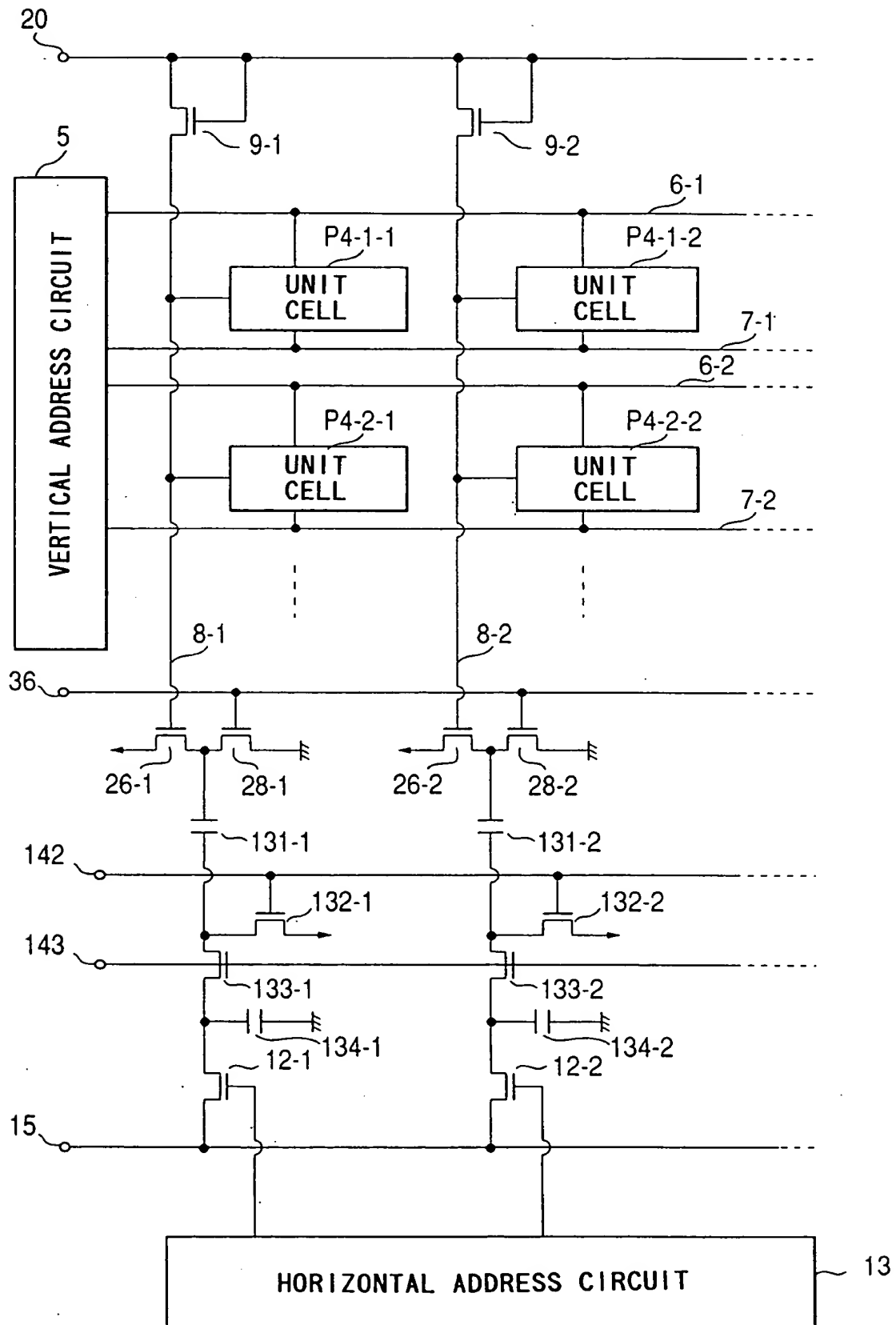


FIG.37

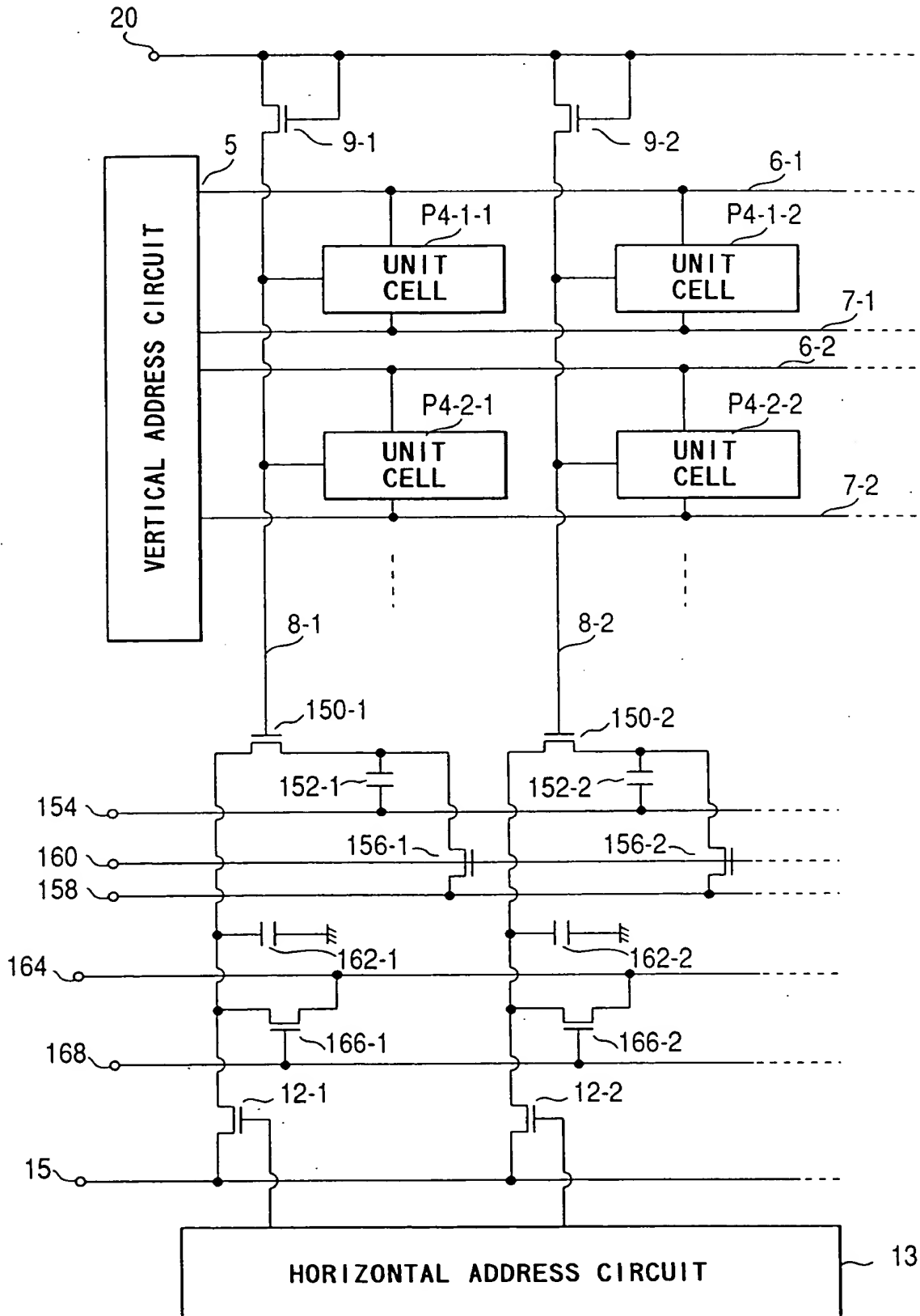


FIG.38

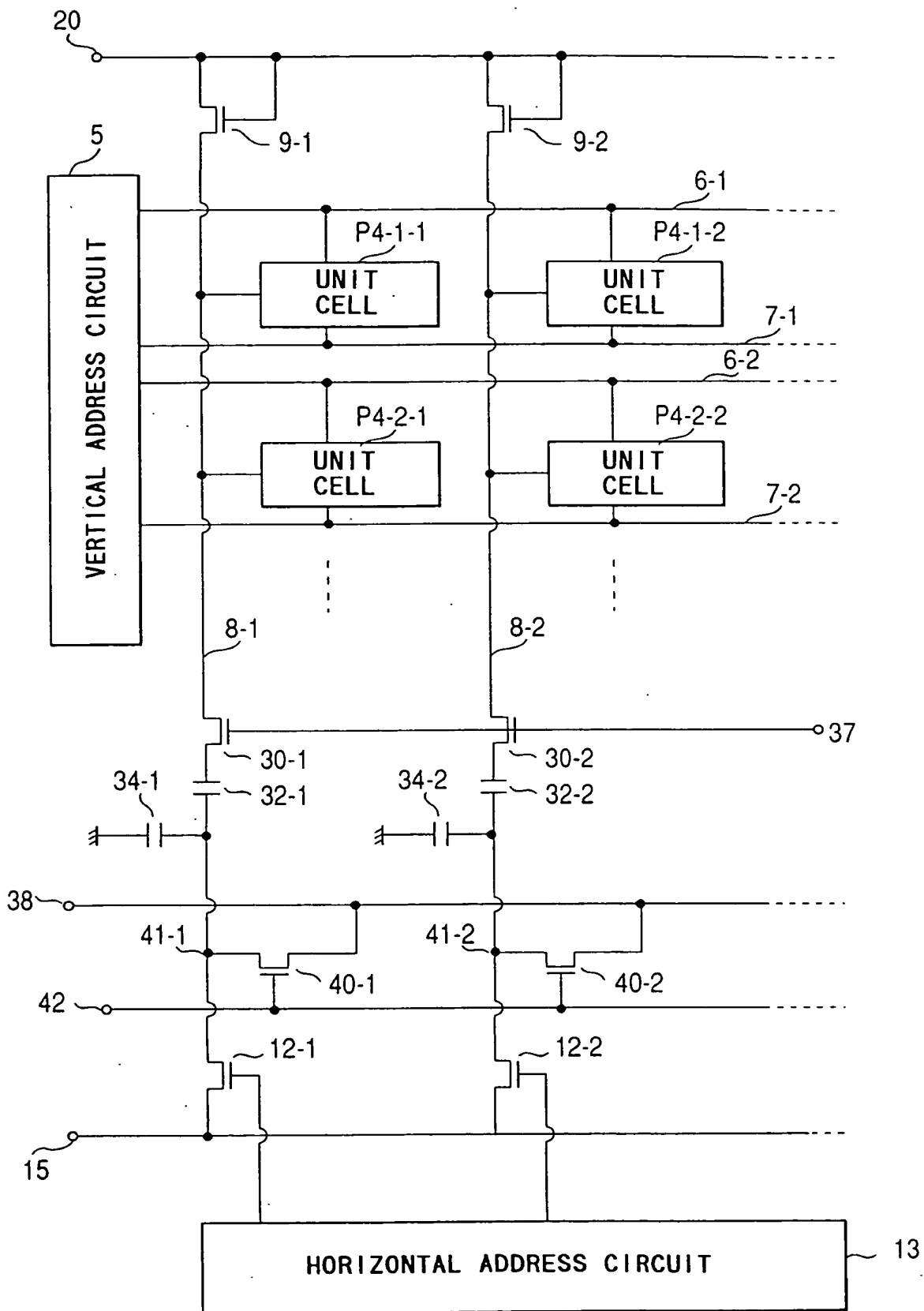


FIG.39

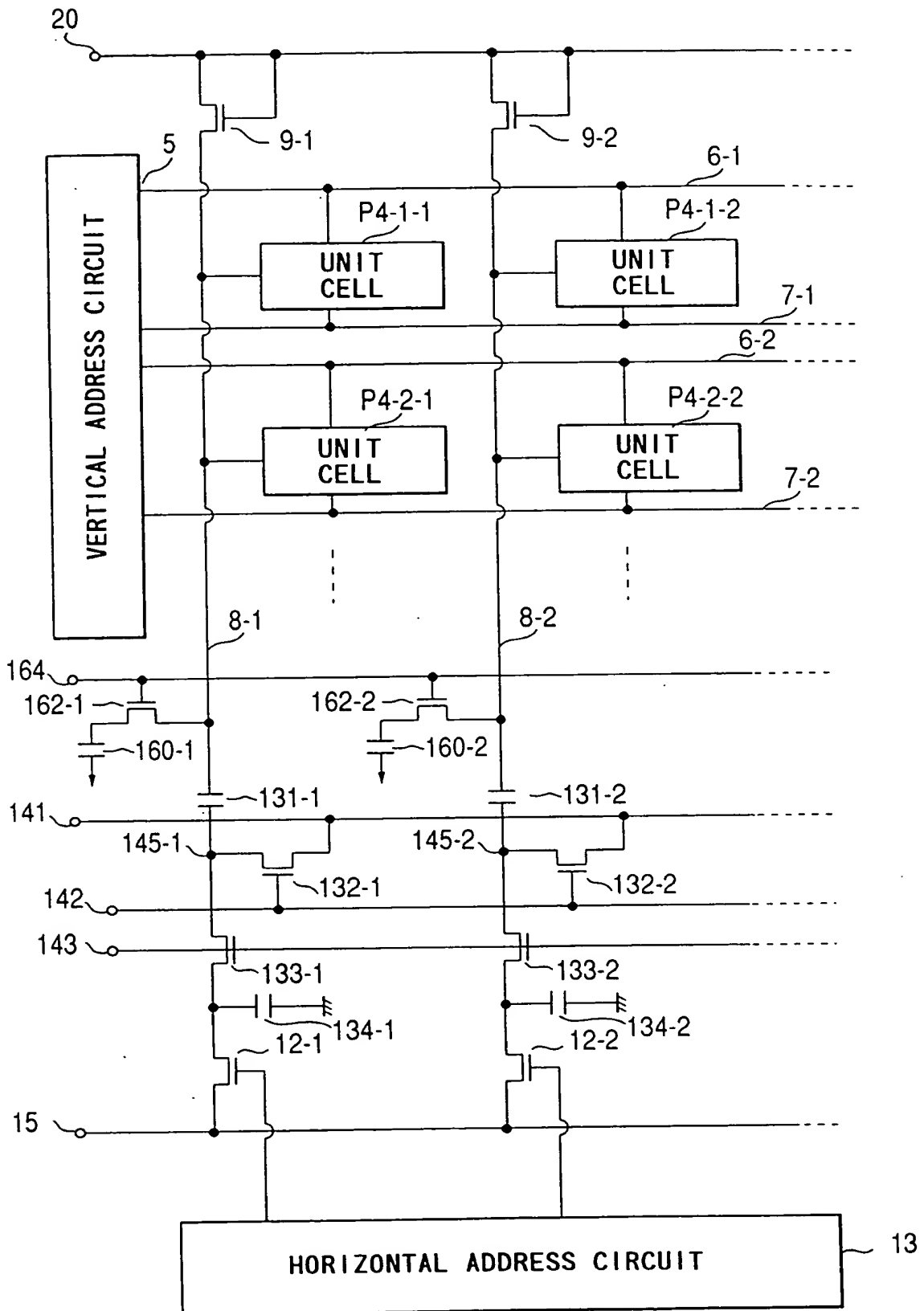


FIG.40

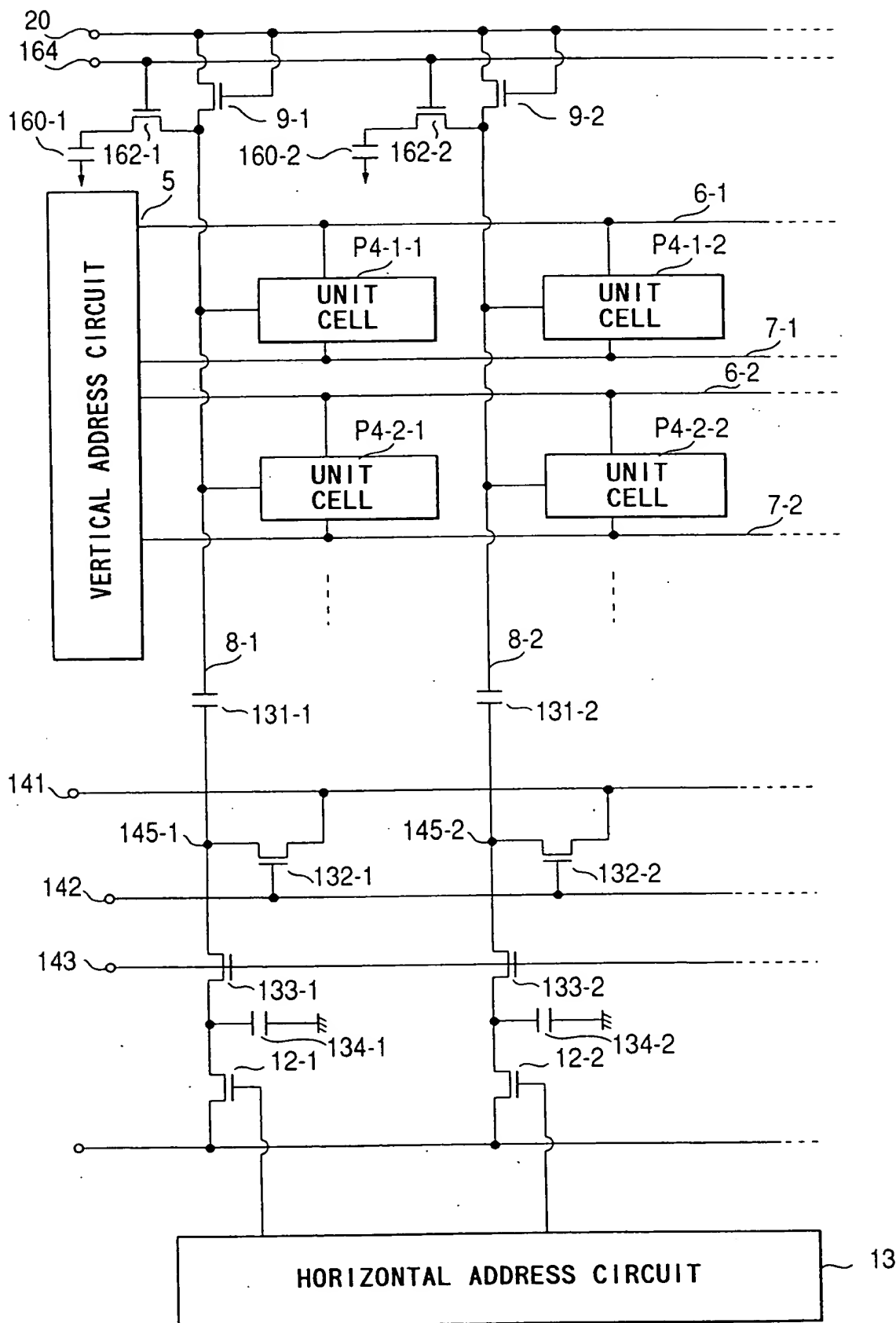


FIG.41

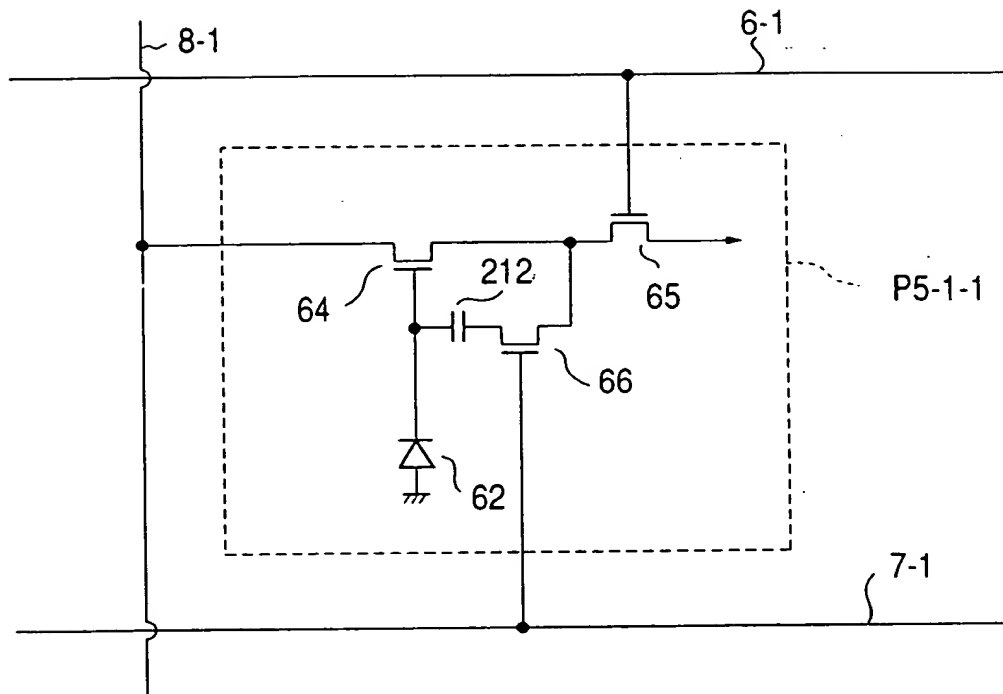


FIG.42

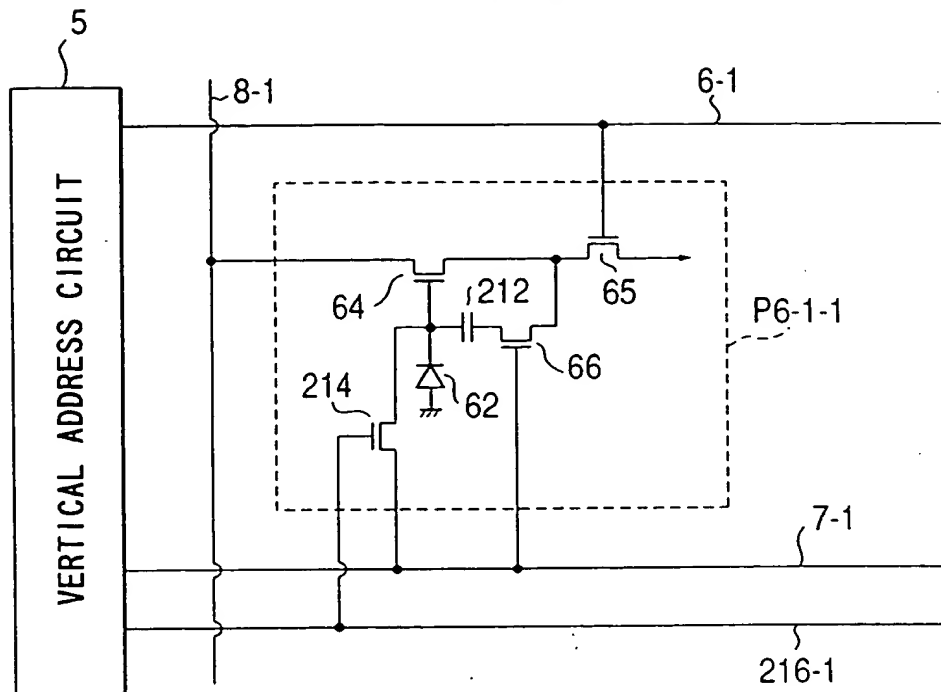


FIG.43

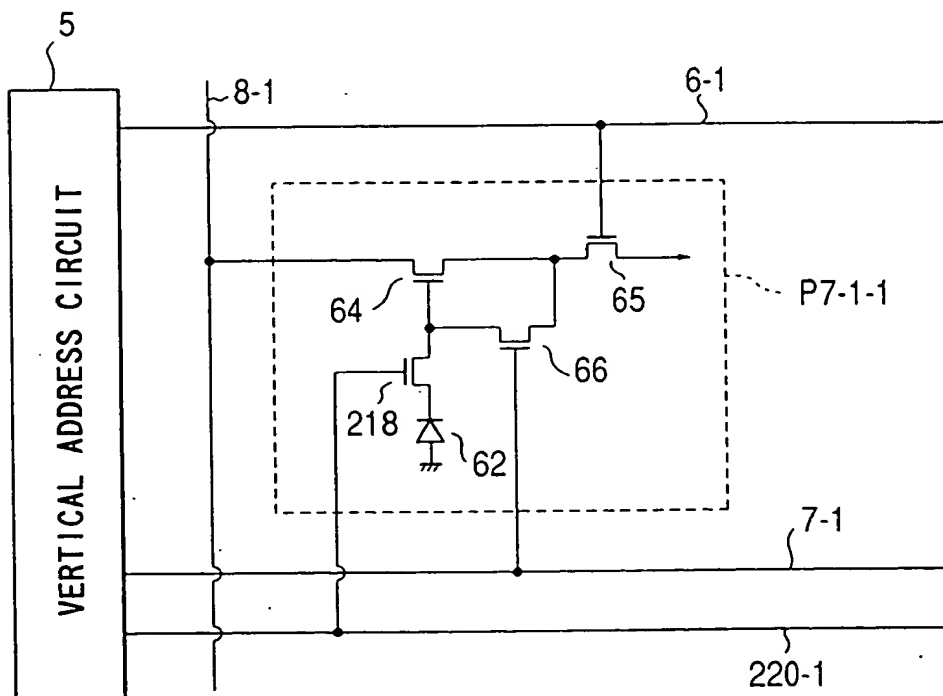


FIG.44

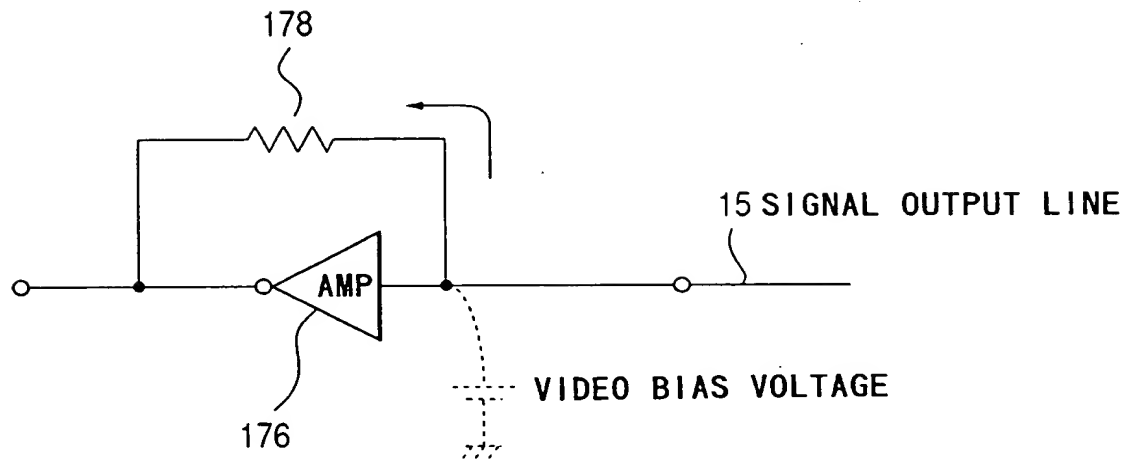


FIG.45

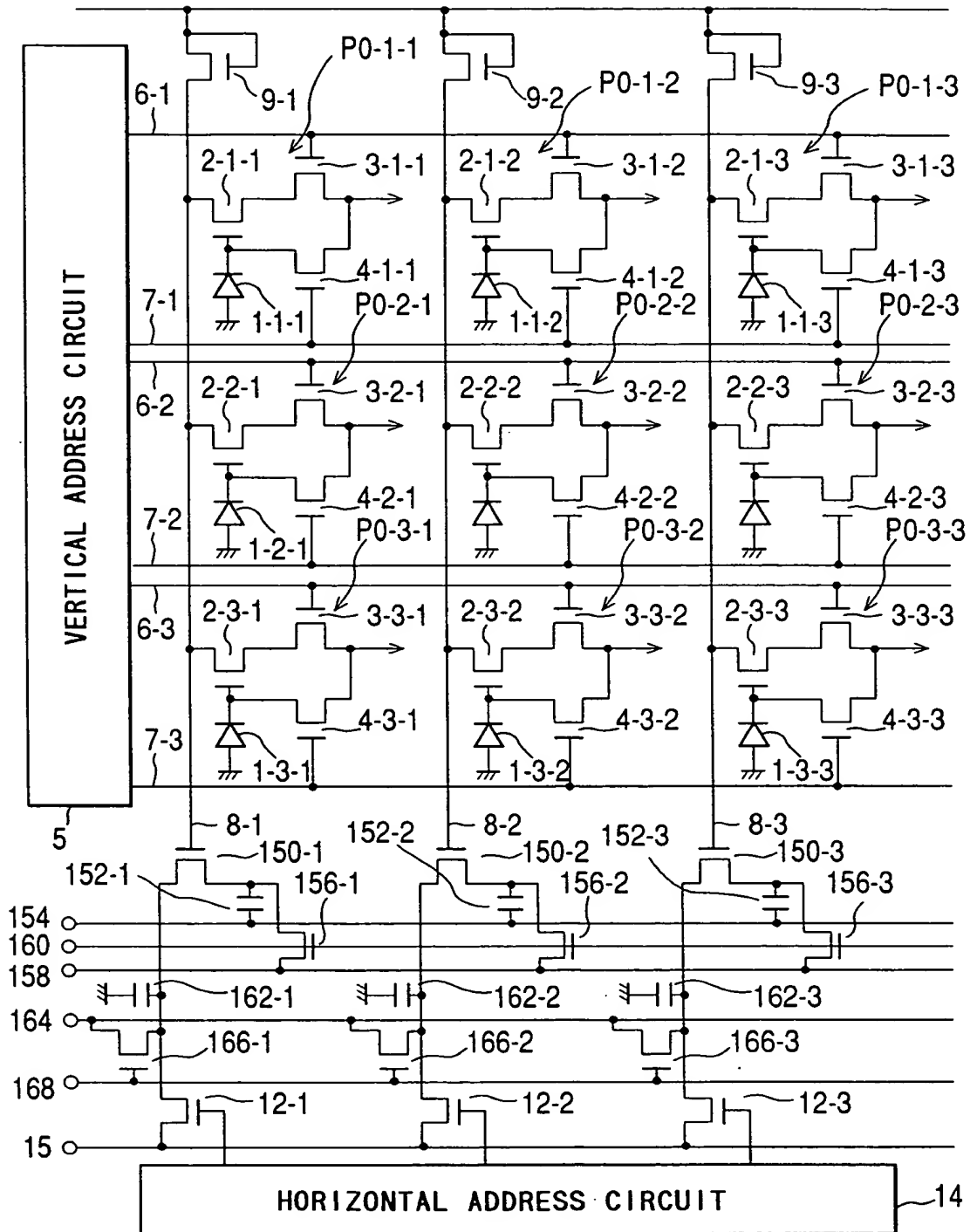


FIG.46

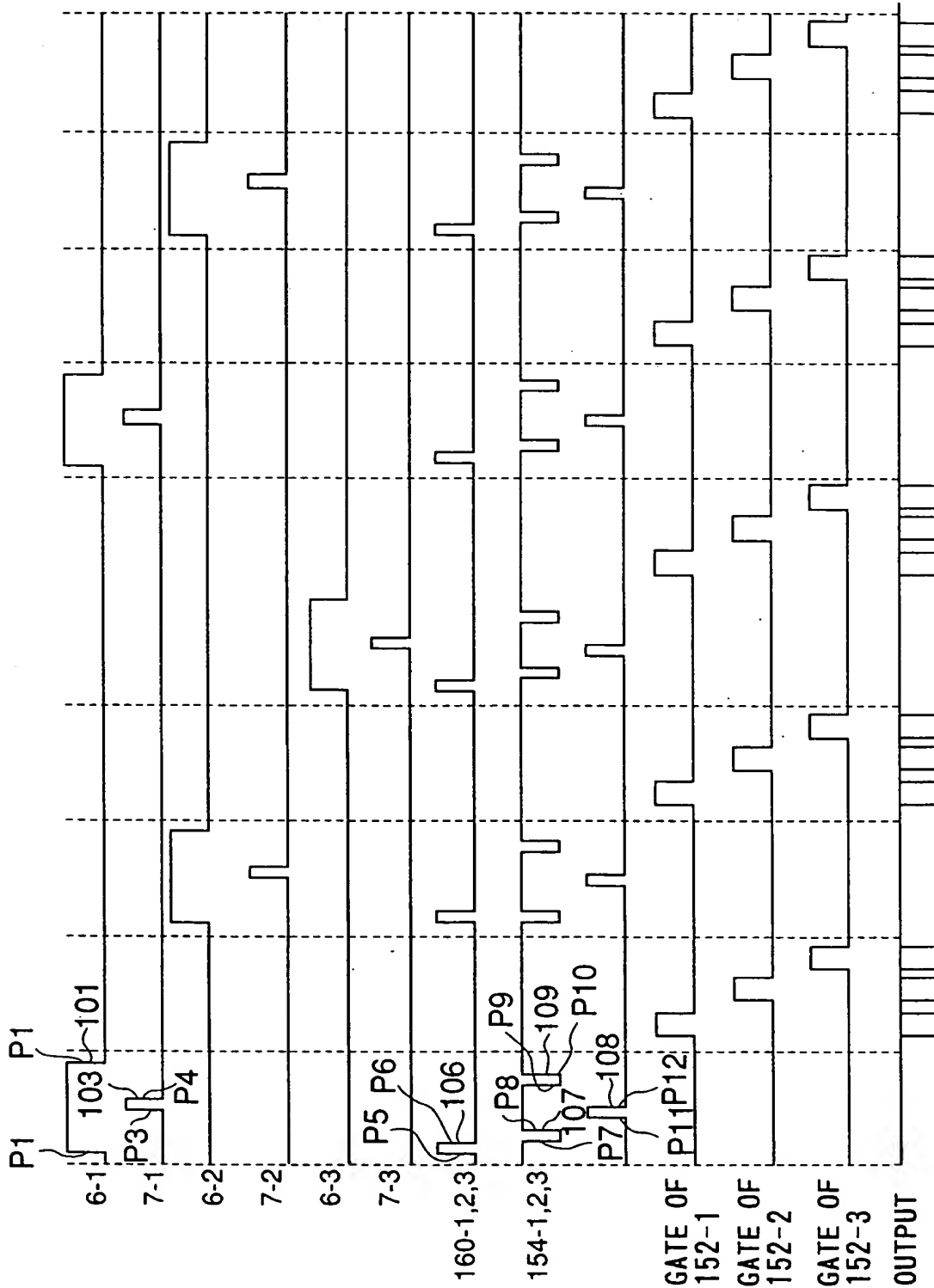


FIG.47

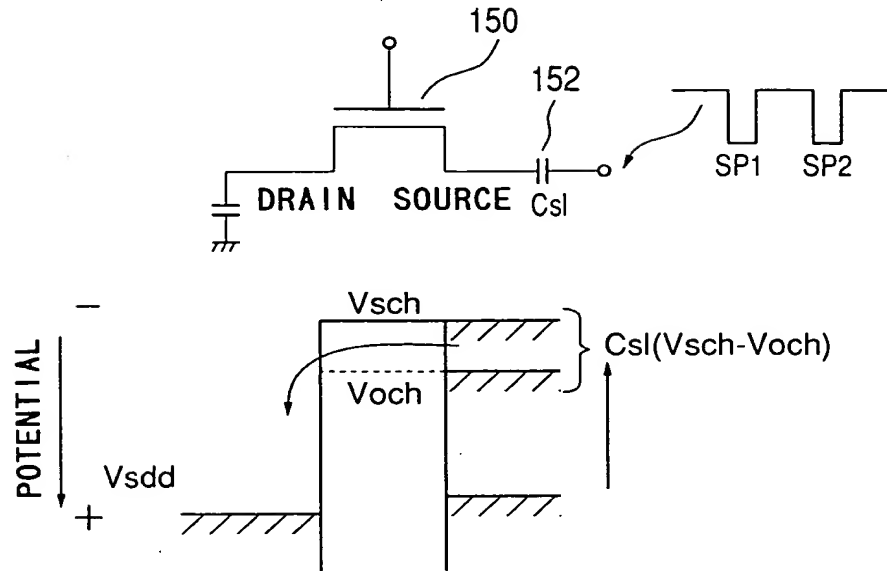


FIG.48

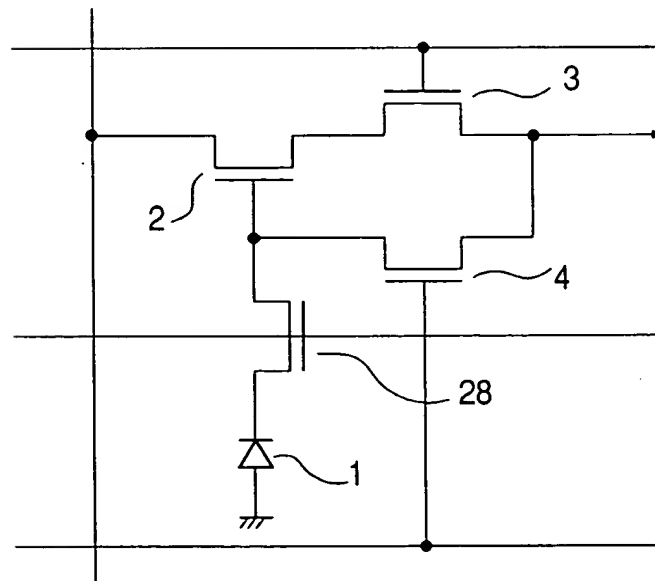


FIG.49

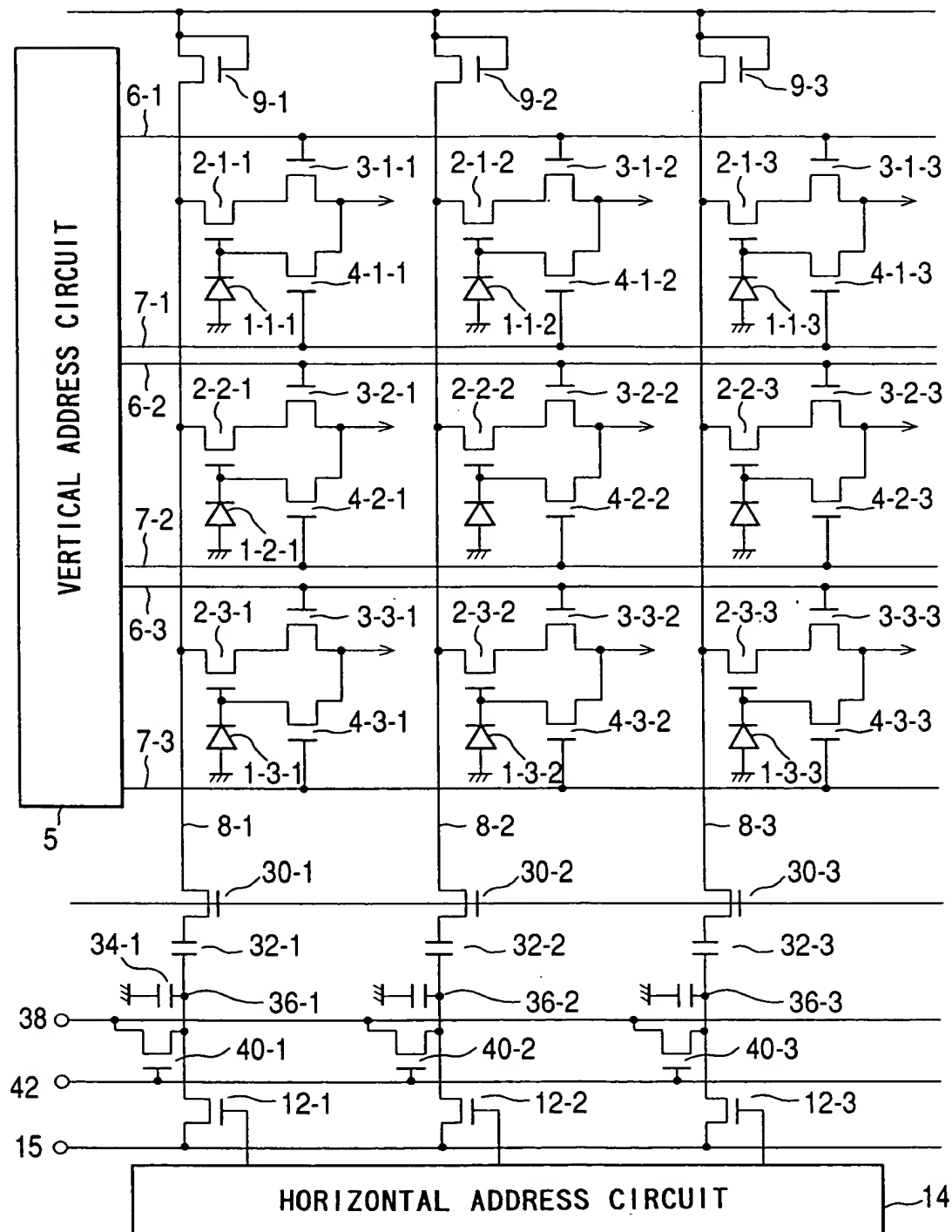


FIG.50

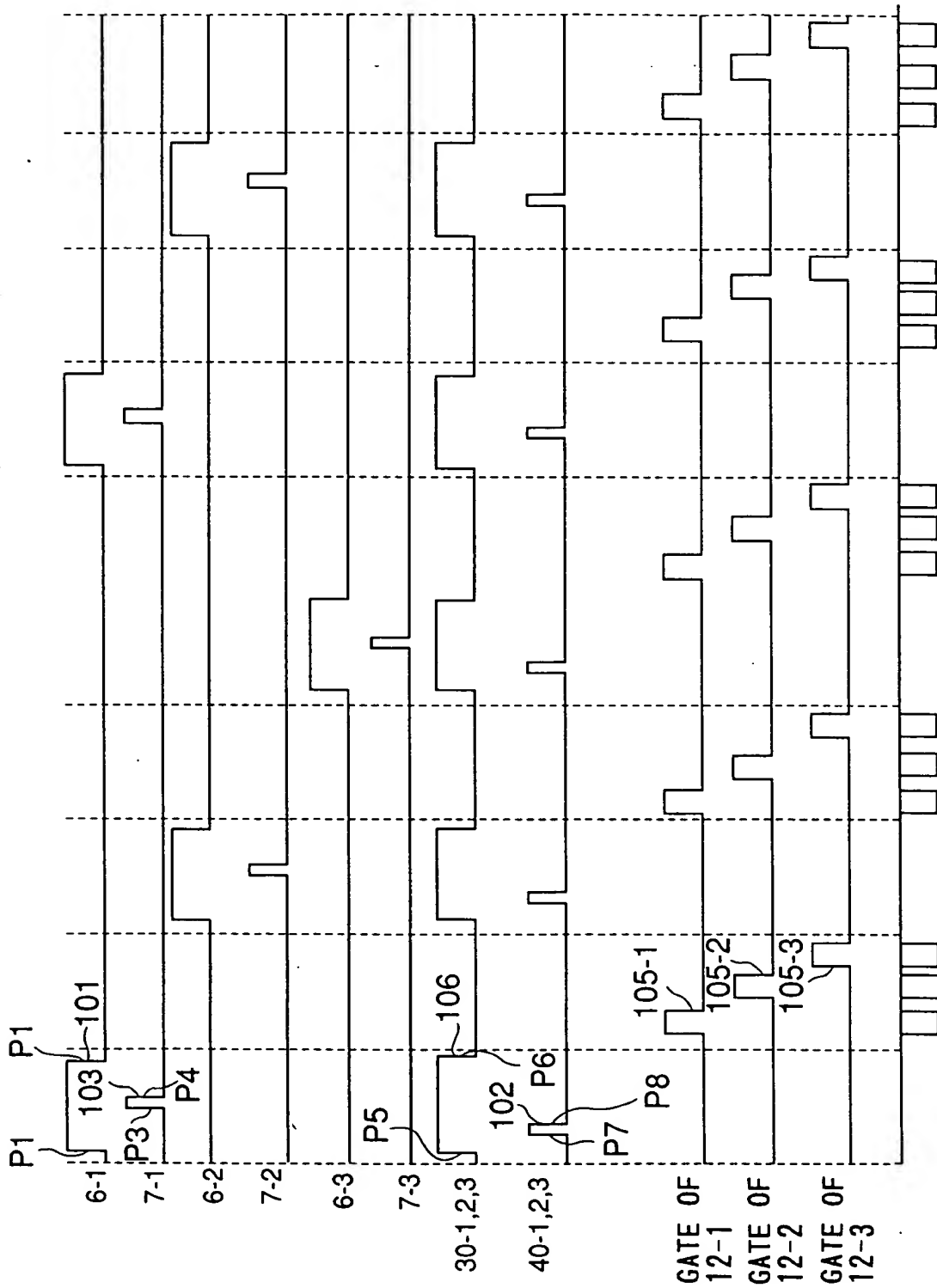


FIG.51





FIG.53

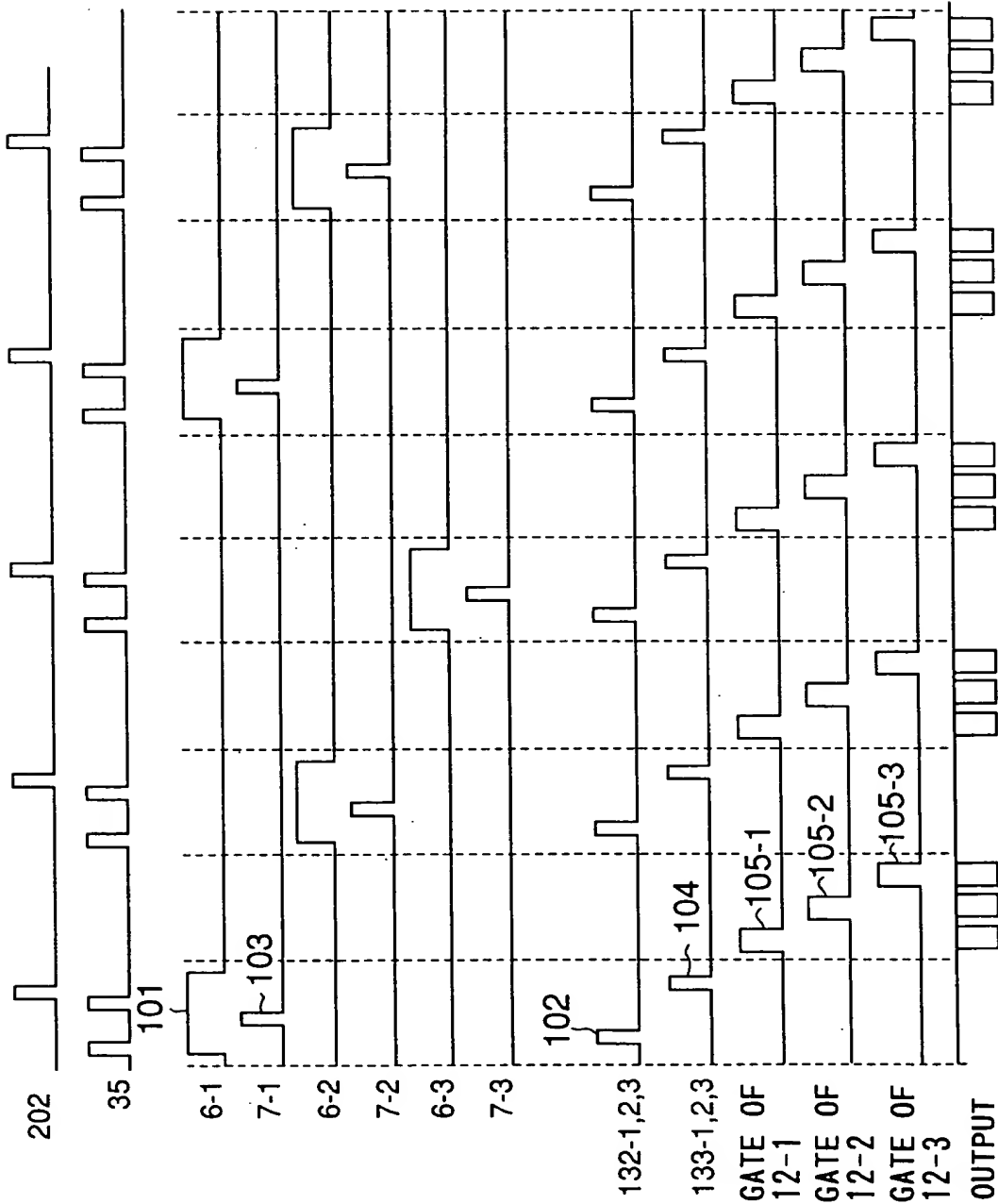


FIG. 54

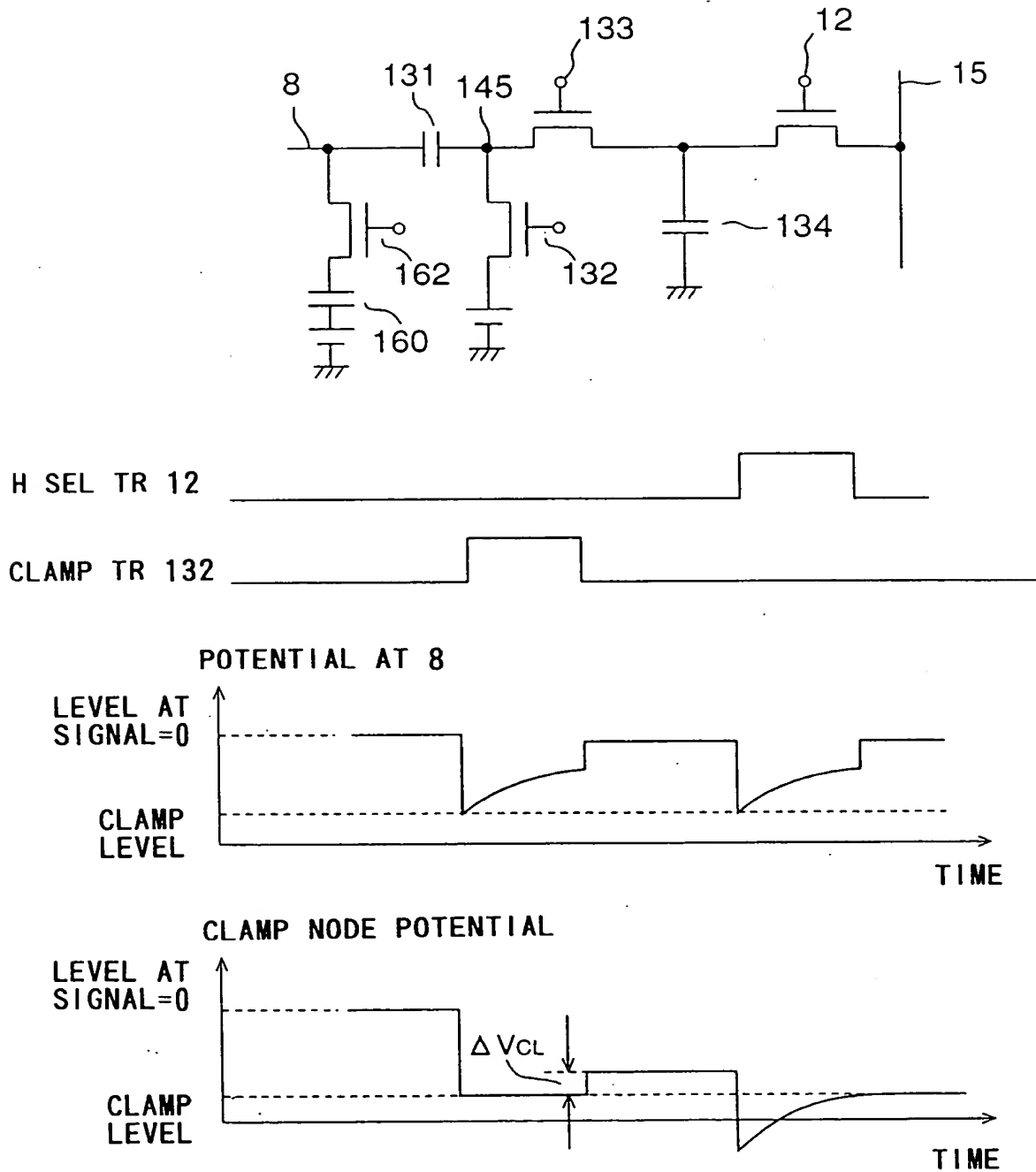
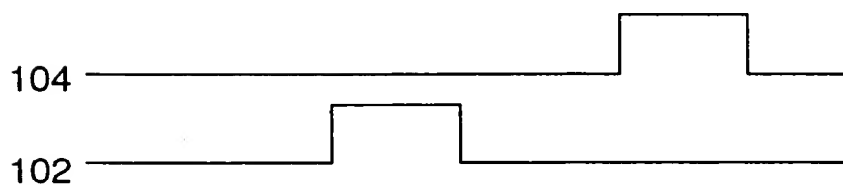


FIG.55



LEVEL AT SIGNAL=0

CLAMP LEVEL

TIME

ΔV_{CL}

FIG.56

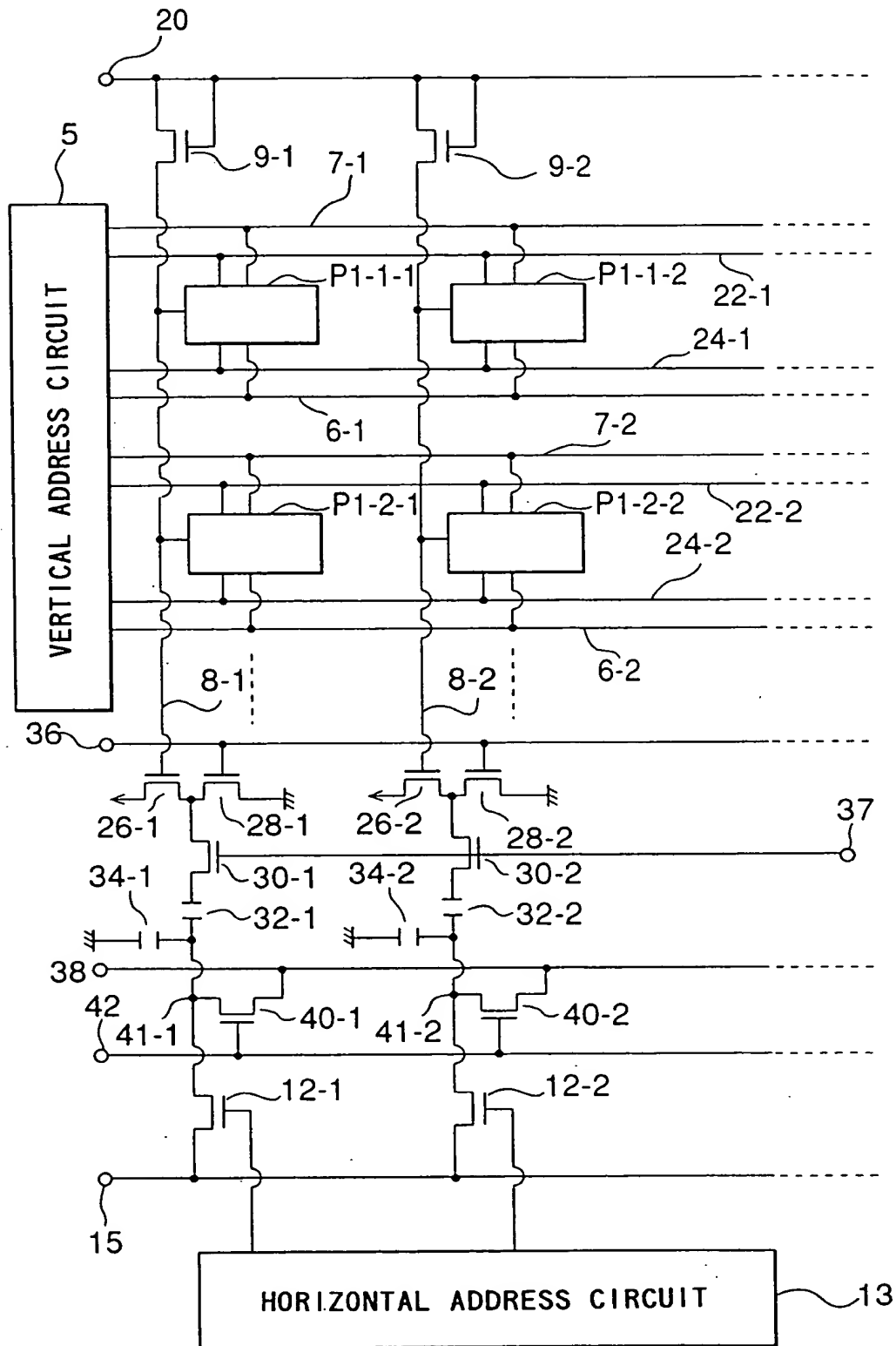


FIG.57

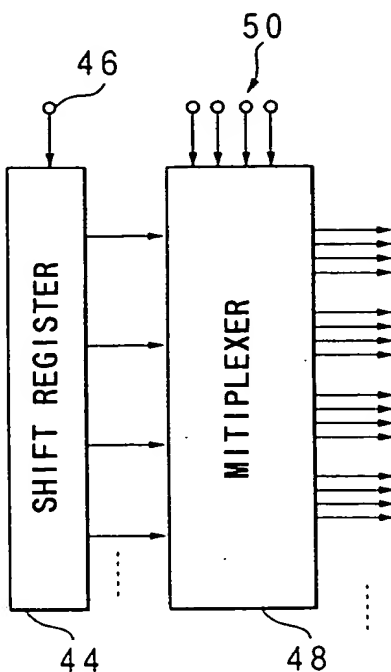


FIG.58

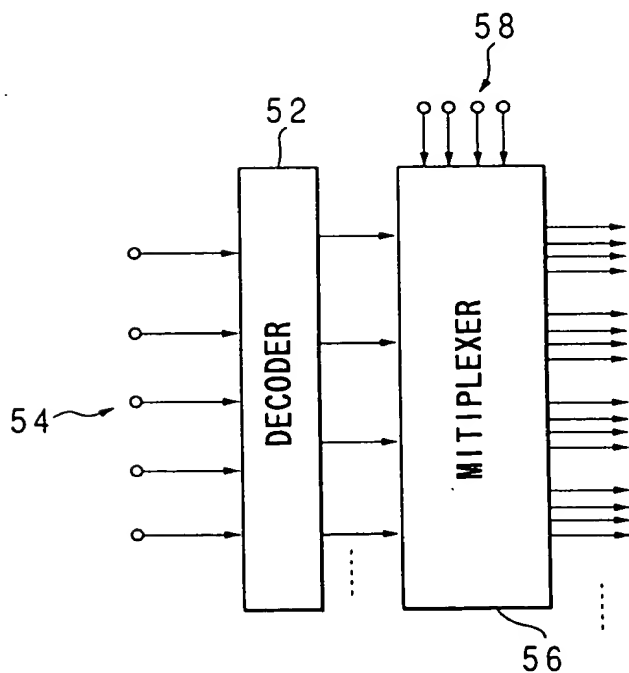


FIG.59

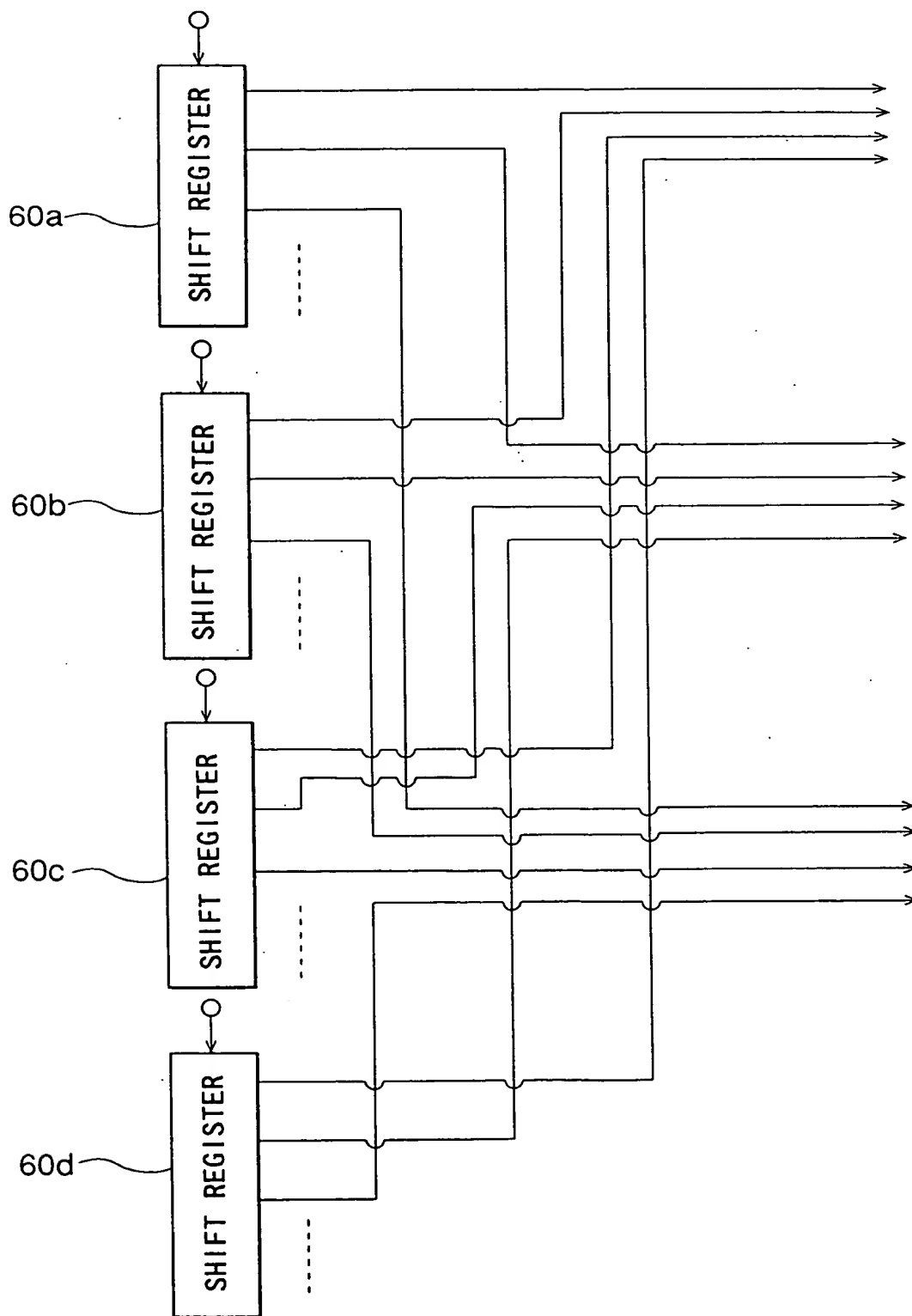


FIG.60

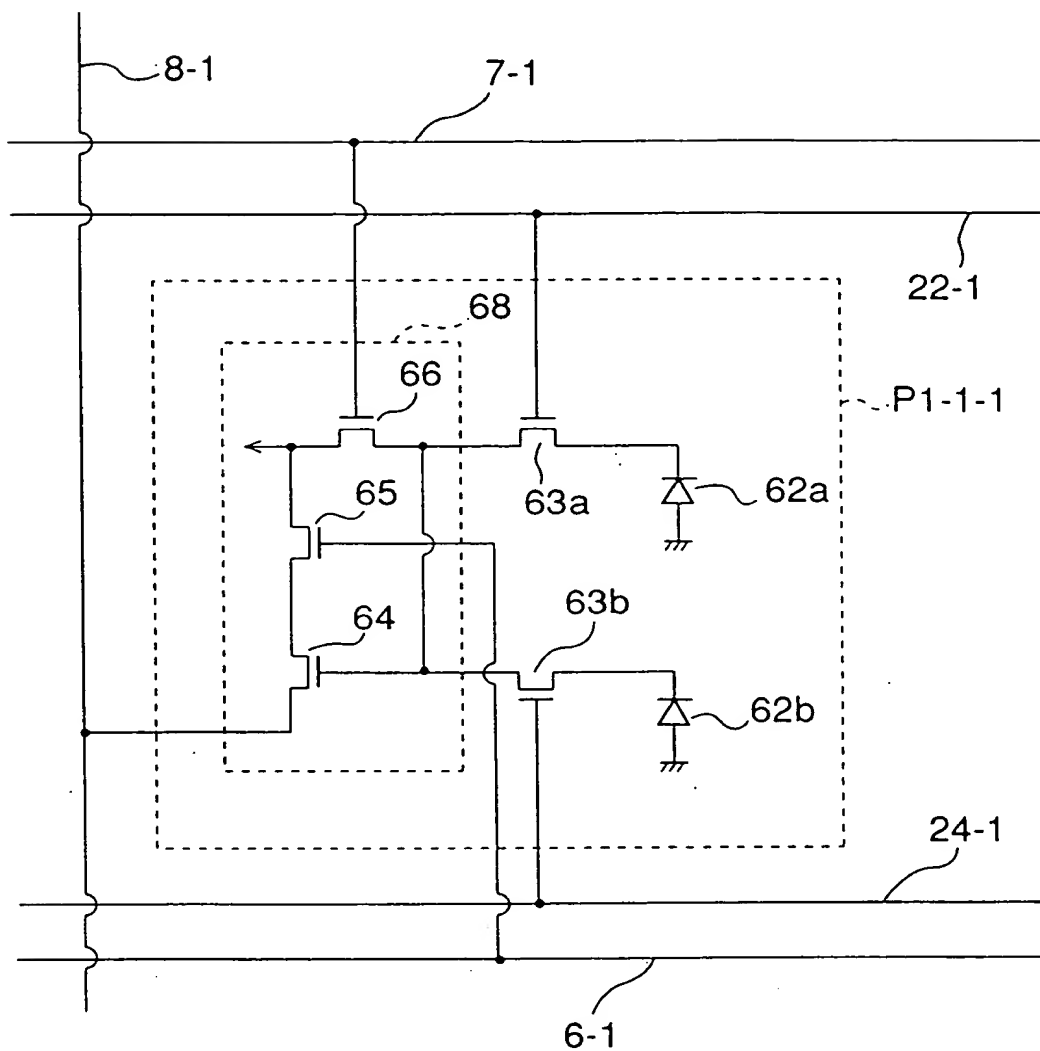


FIG.61

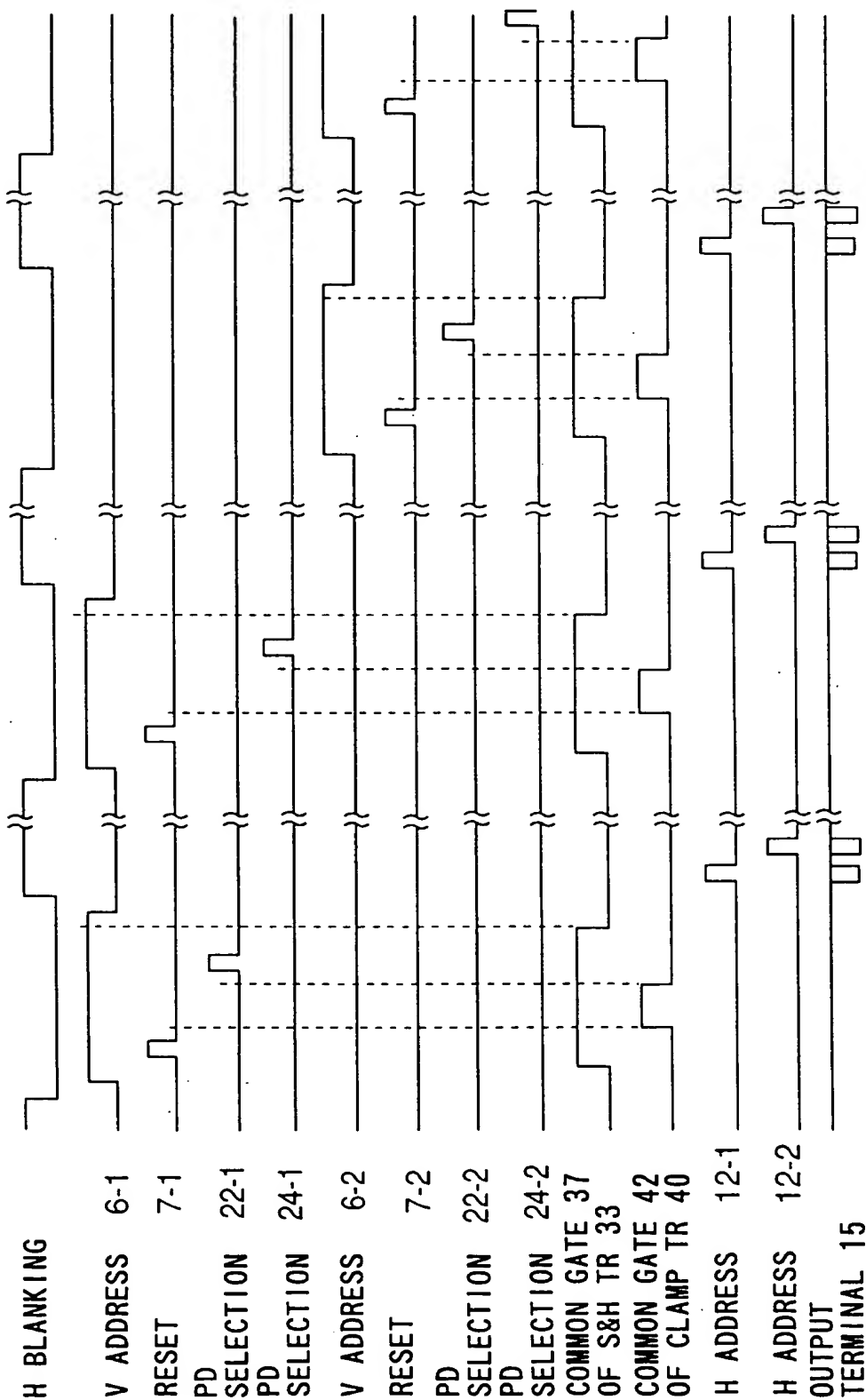


FIG.62

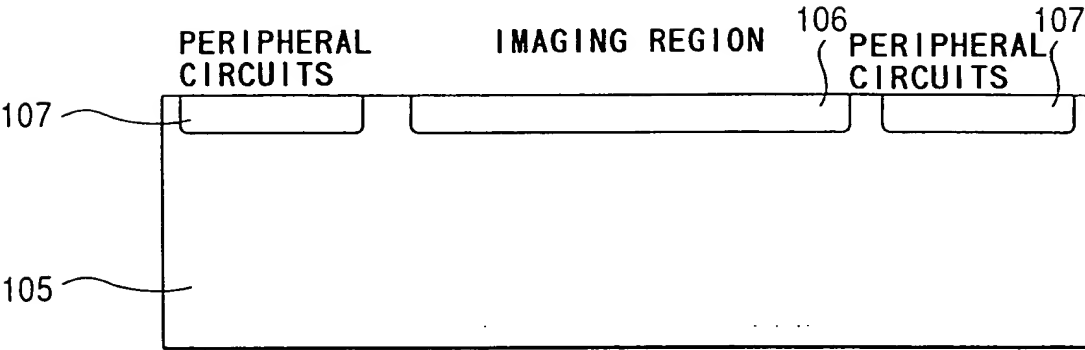


FIG.63

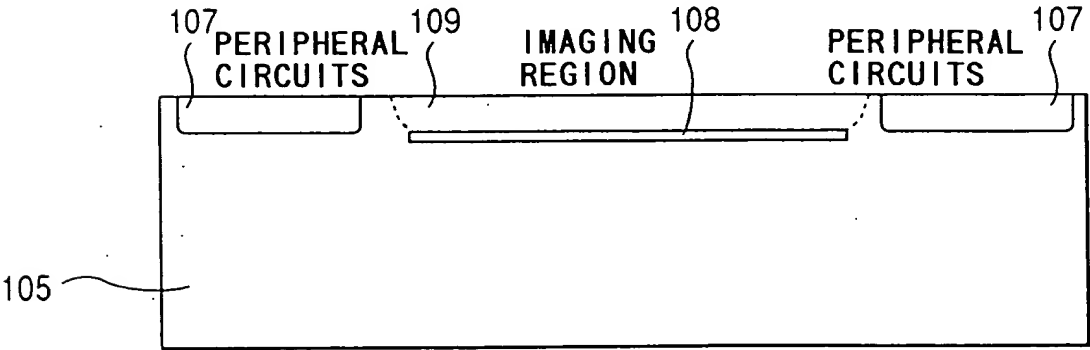


FIG.64

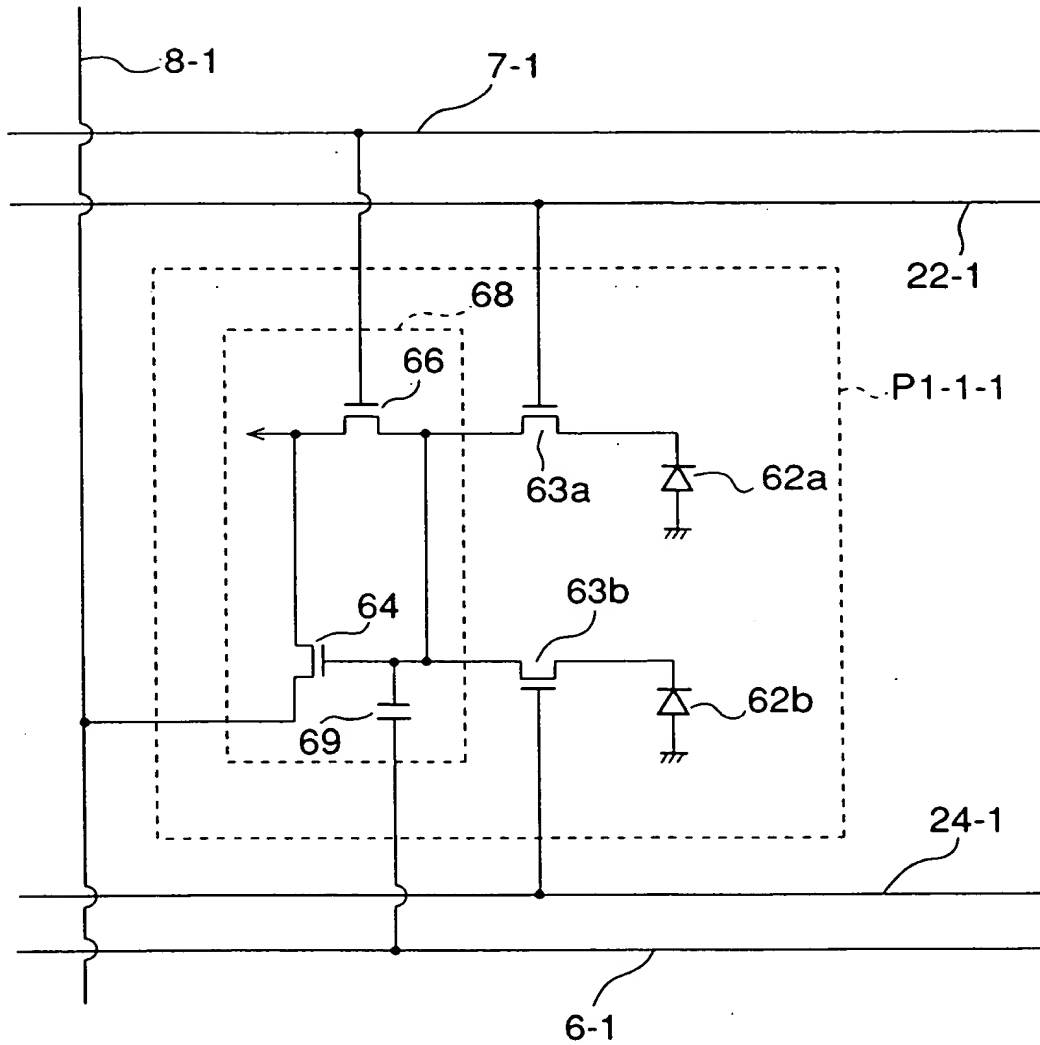


FIG.65

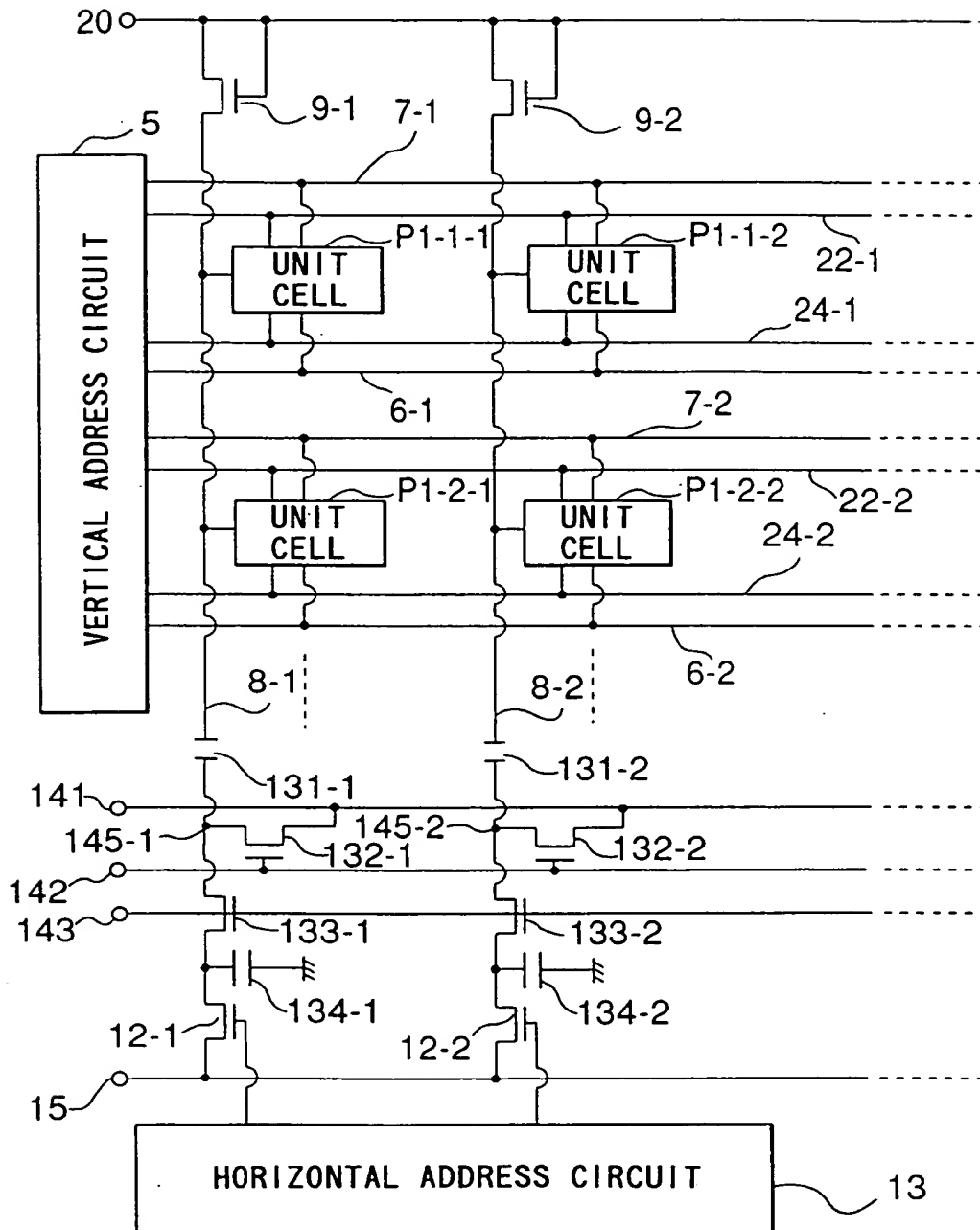


FIG.66

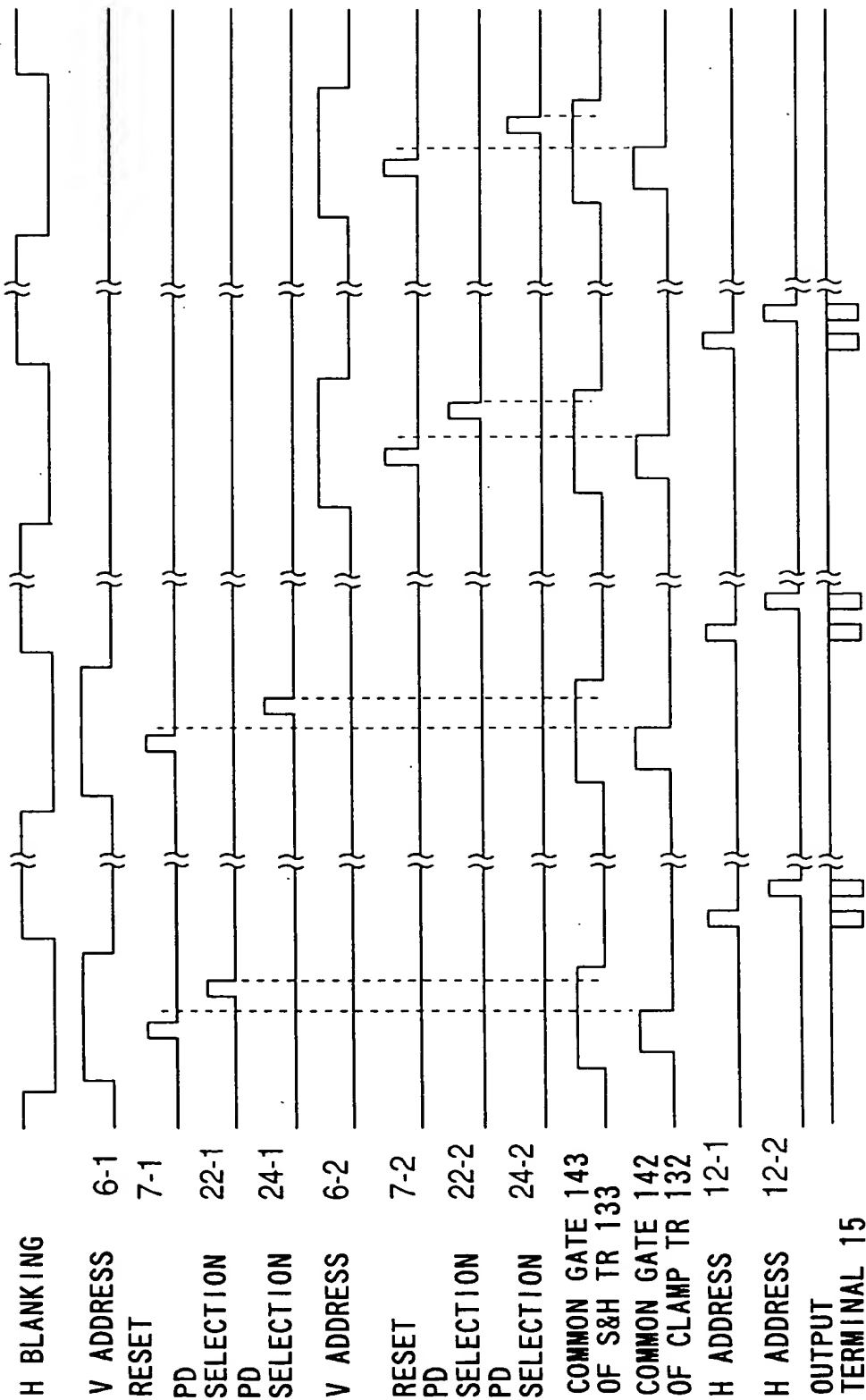


FIG. 67

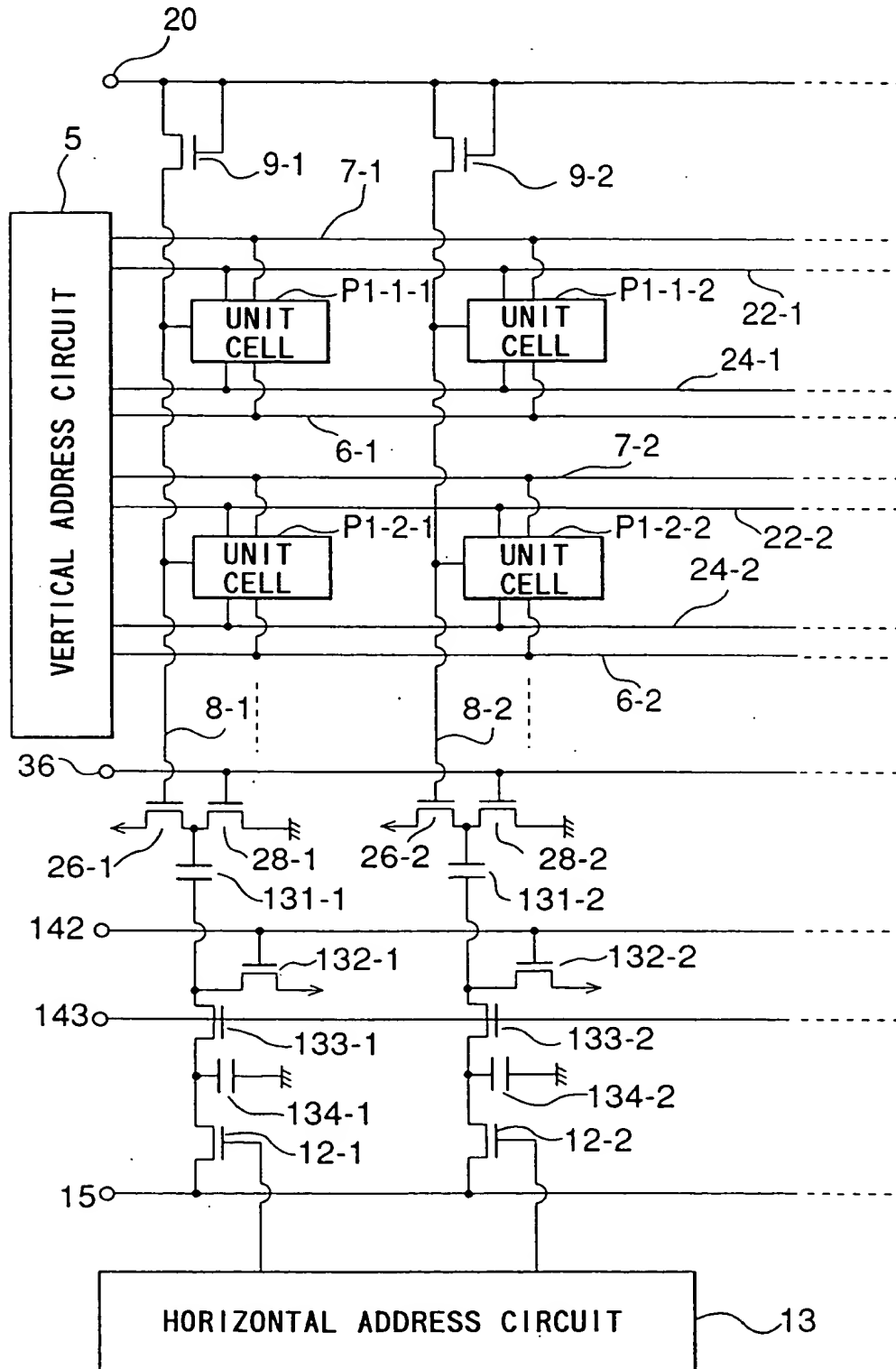


FIG.68

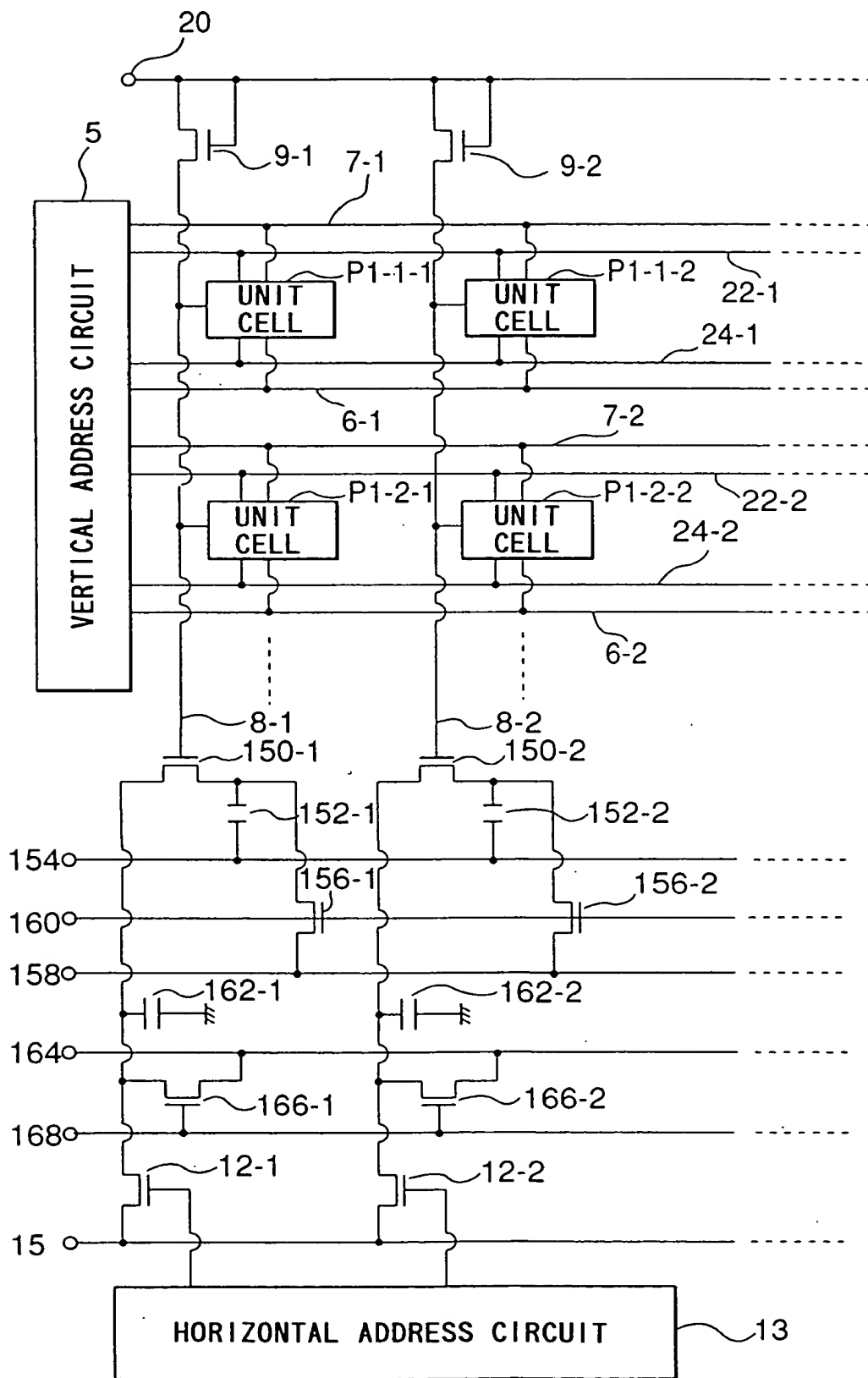


FIG.69

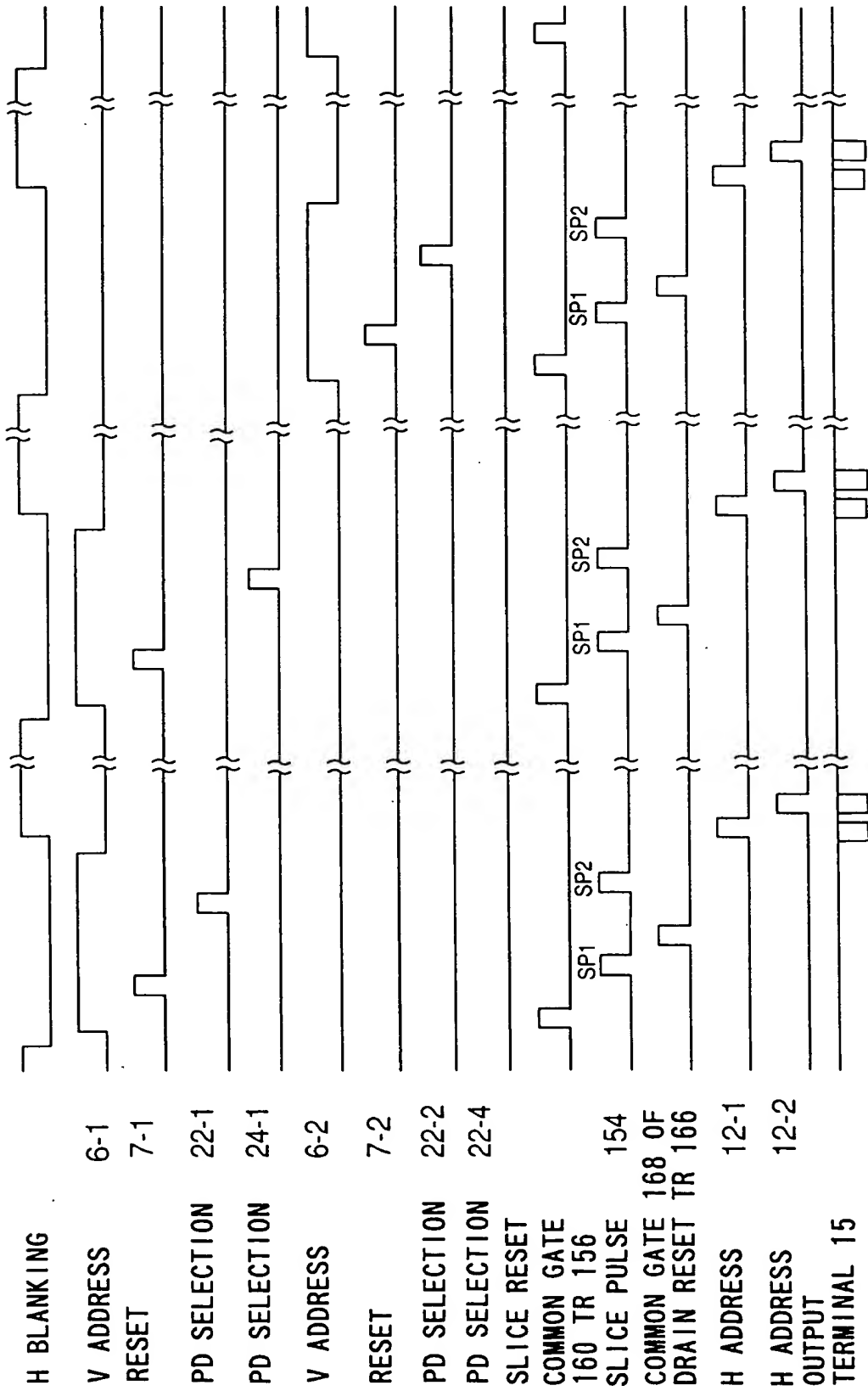


FIG.70

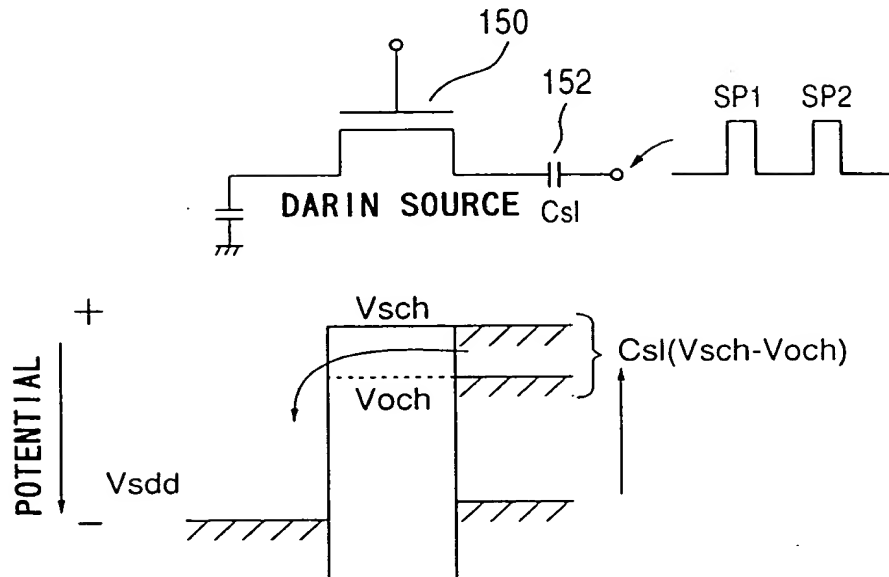


FIG.71

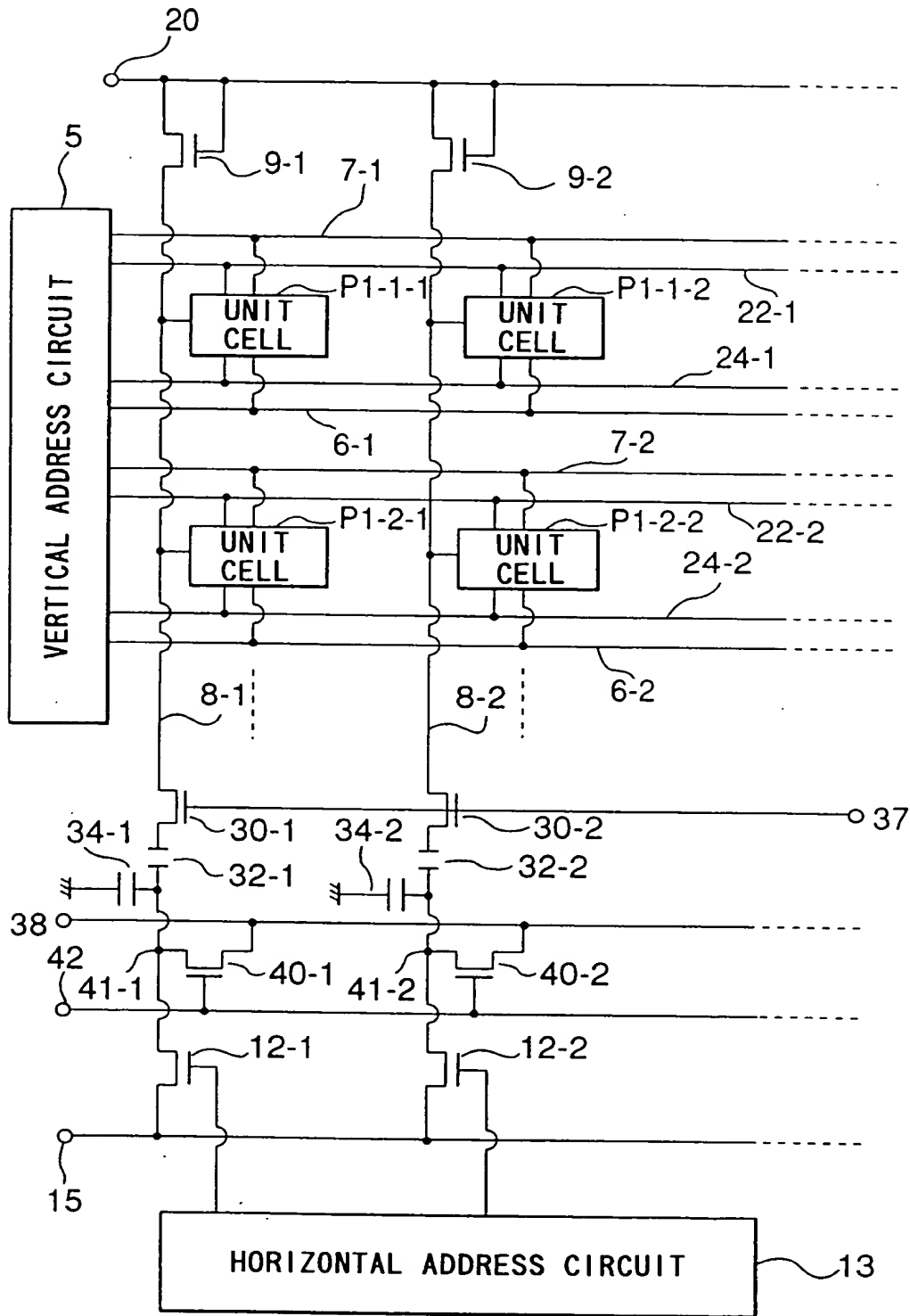


FIG.72

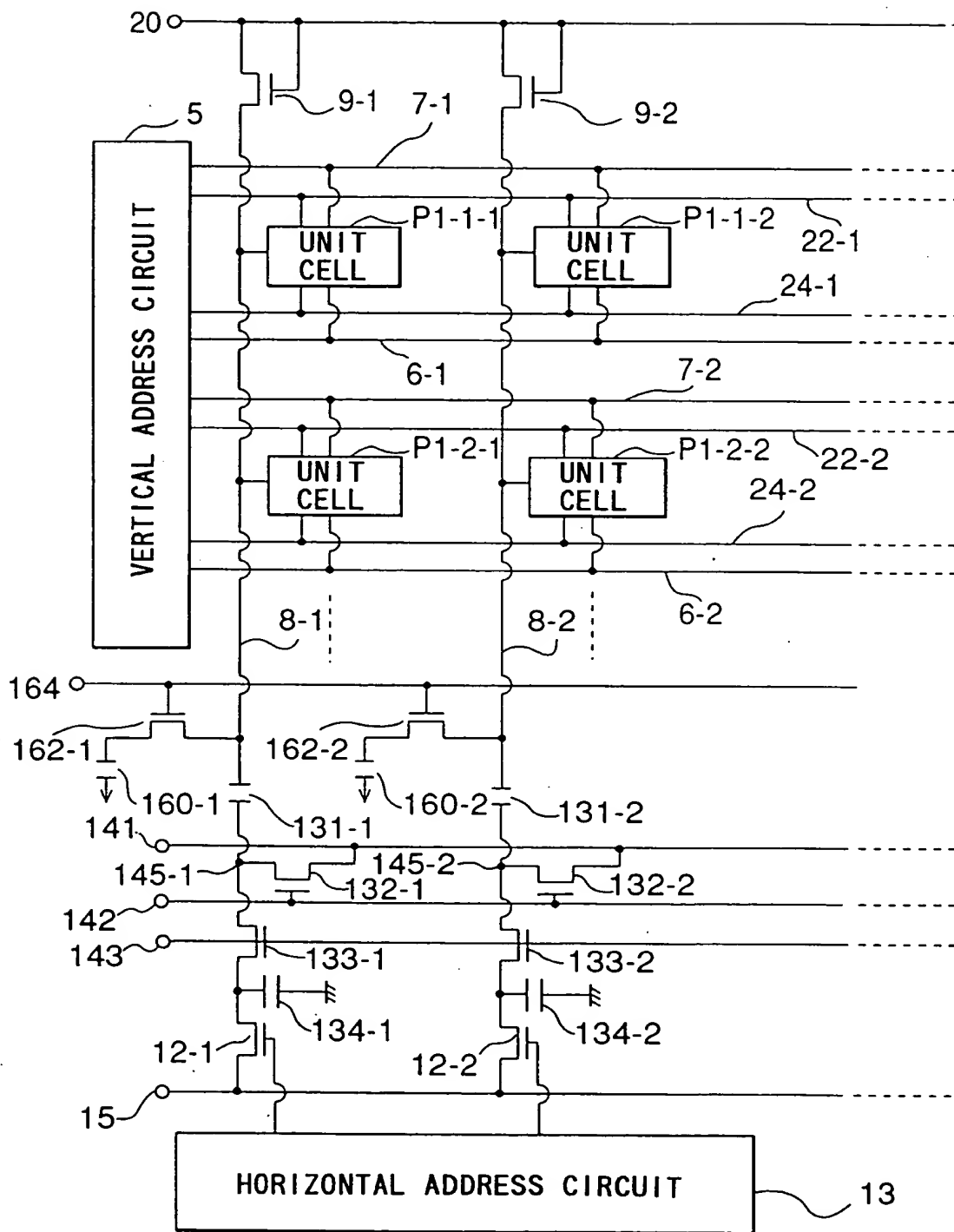


FIG.73

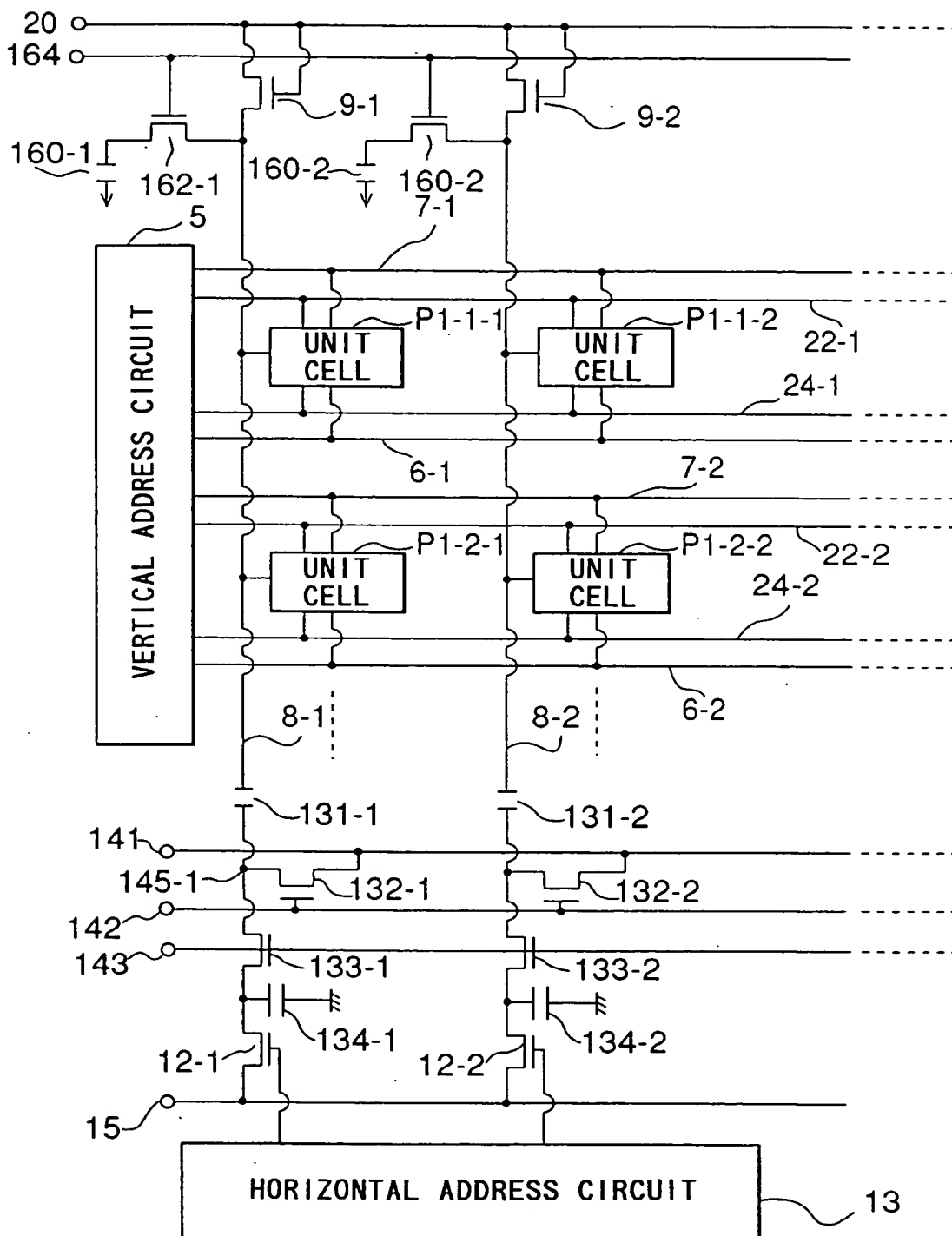


FIG.74

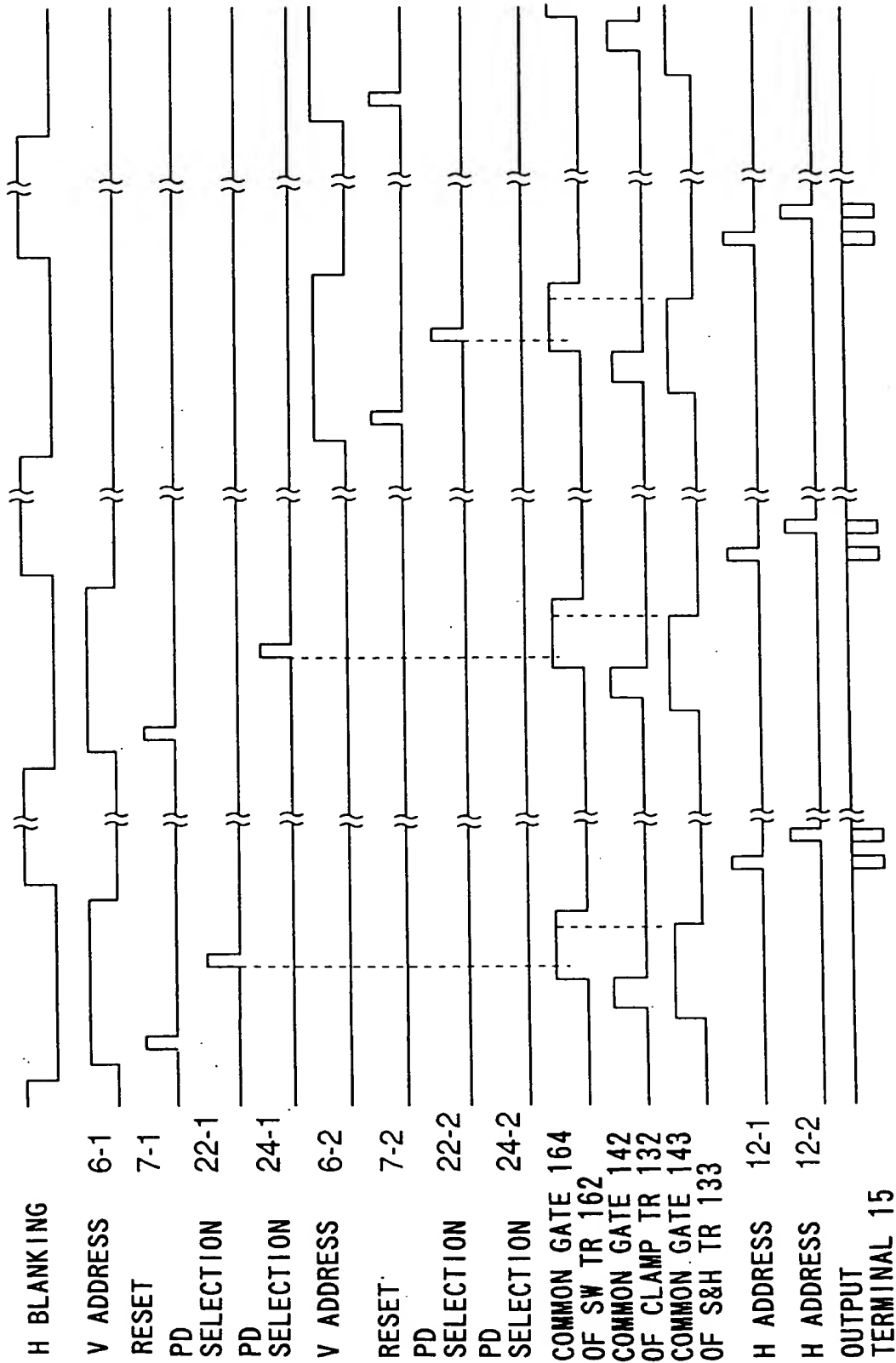


FIG. 75

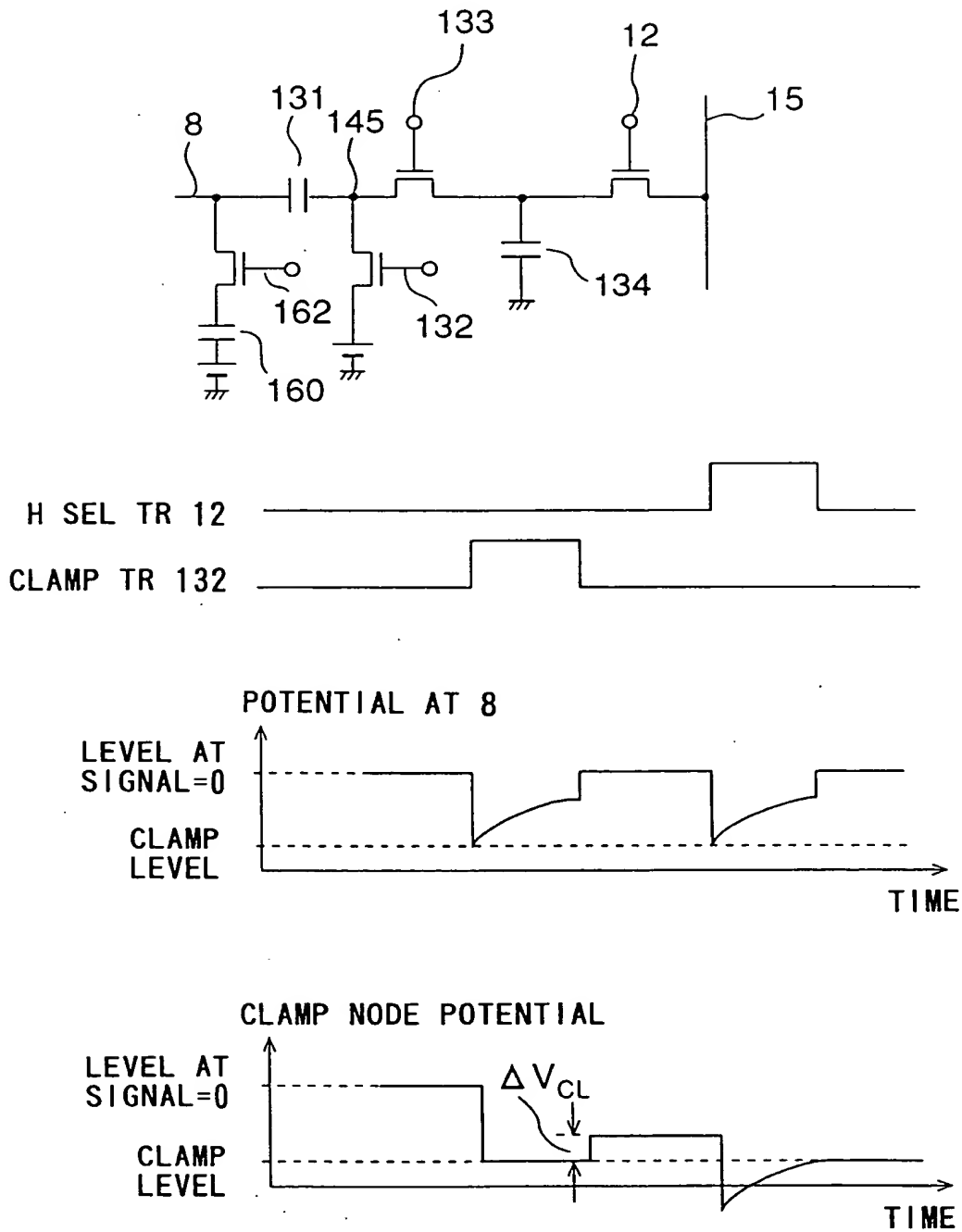


FIG.76

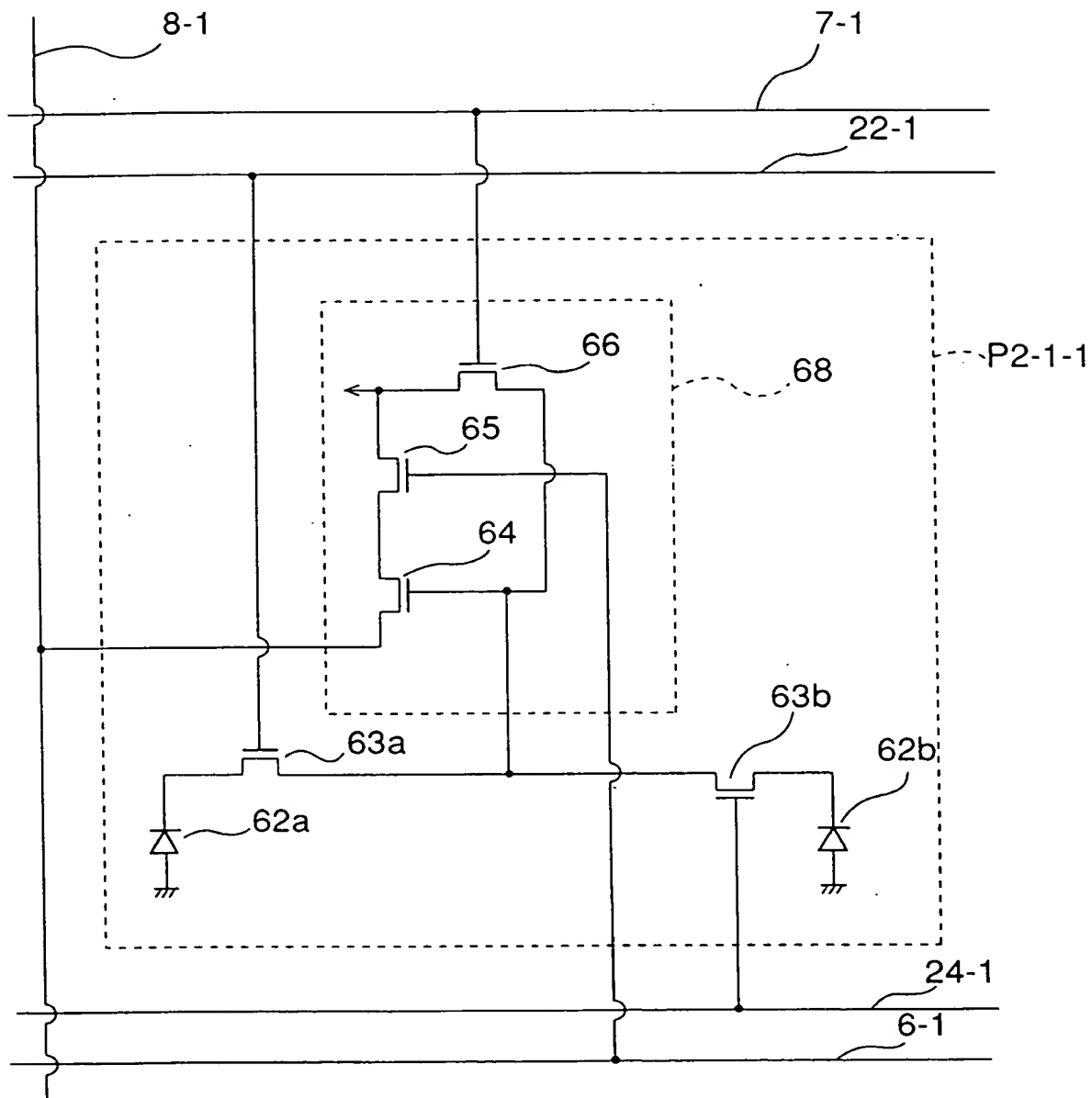


FIG.77

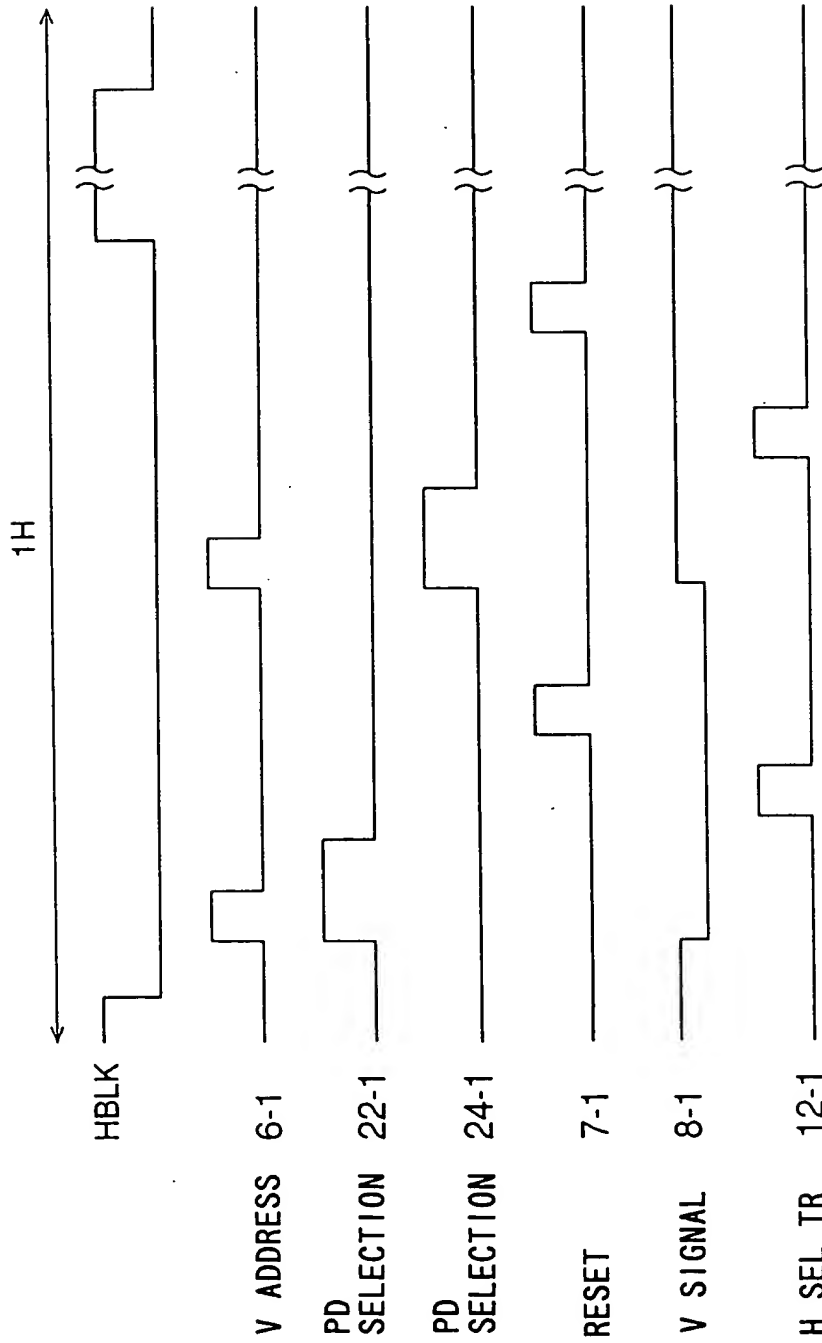


FIG.78

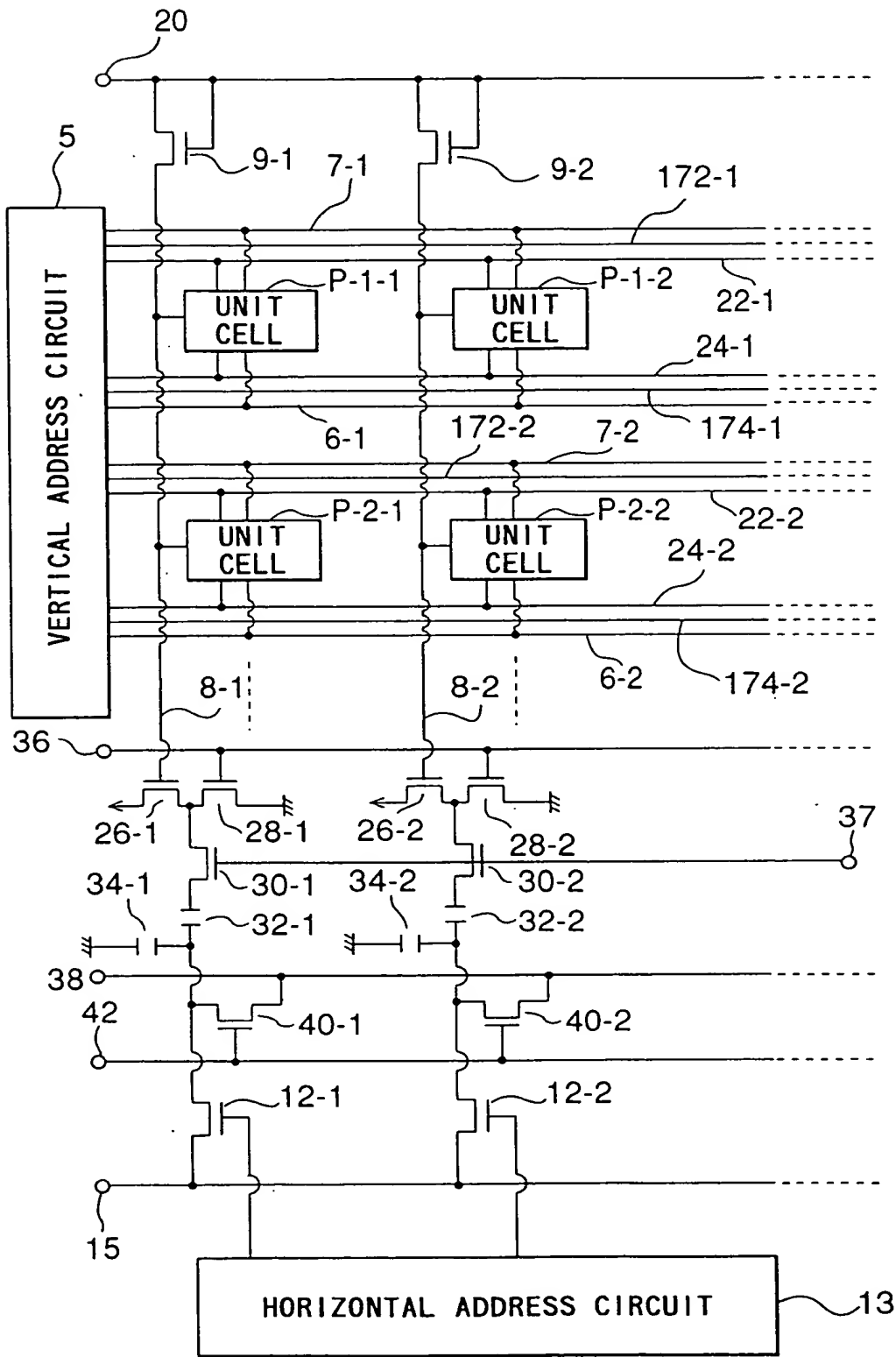


FIG.79

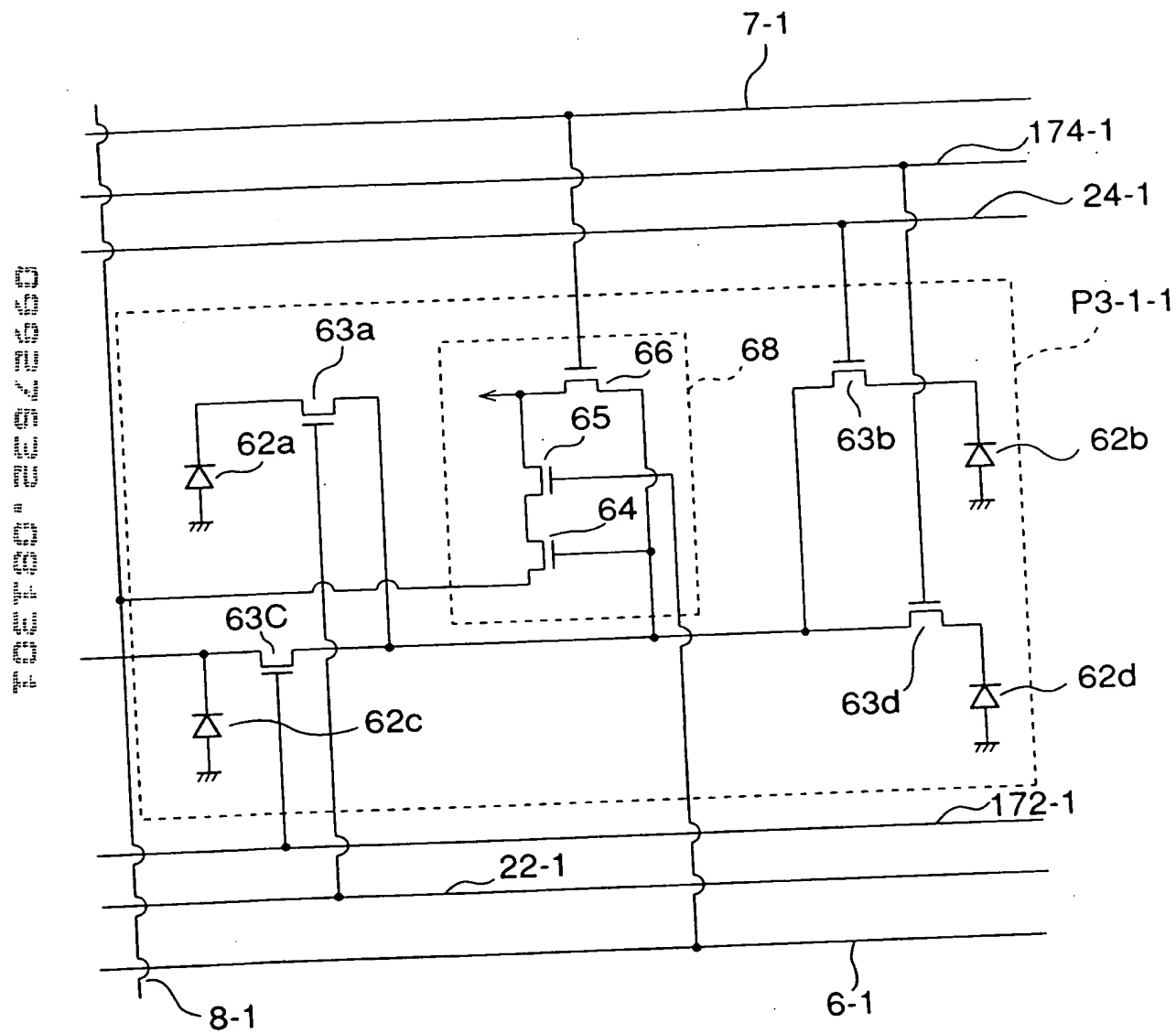


FIG.80

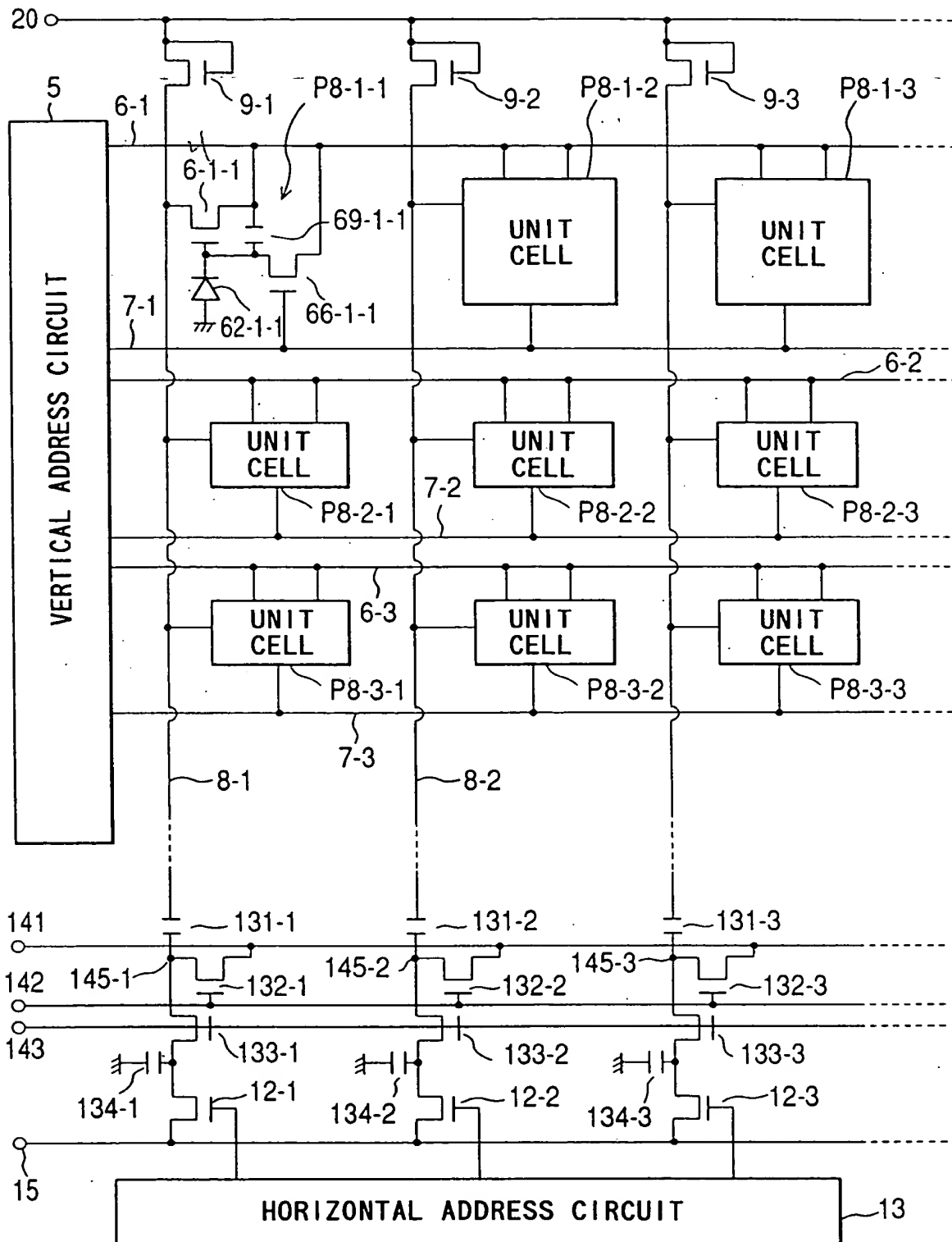


FIG.81

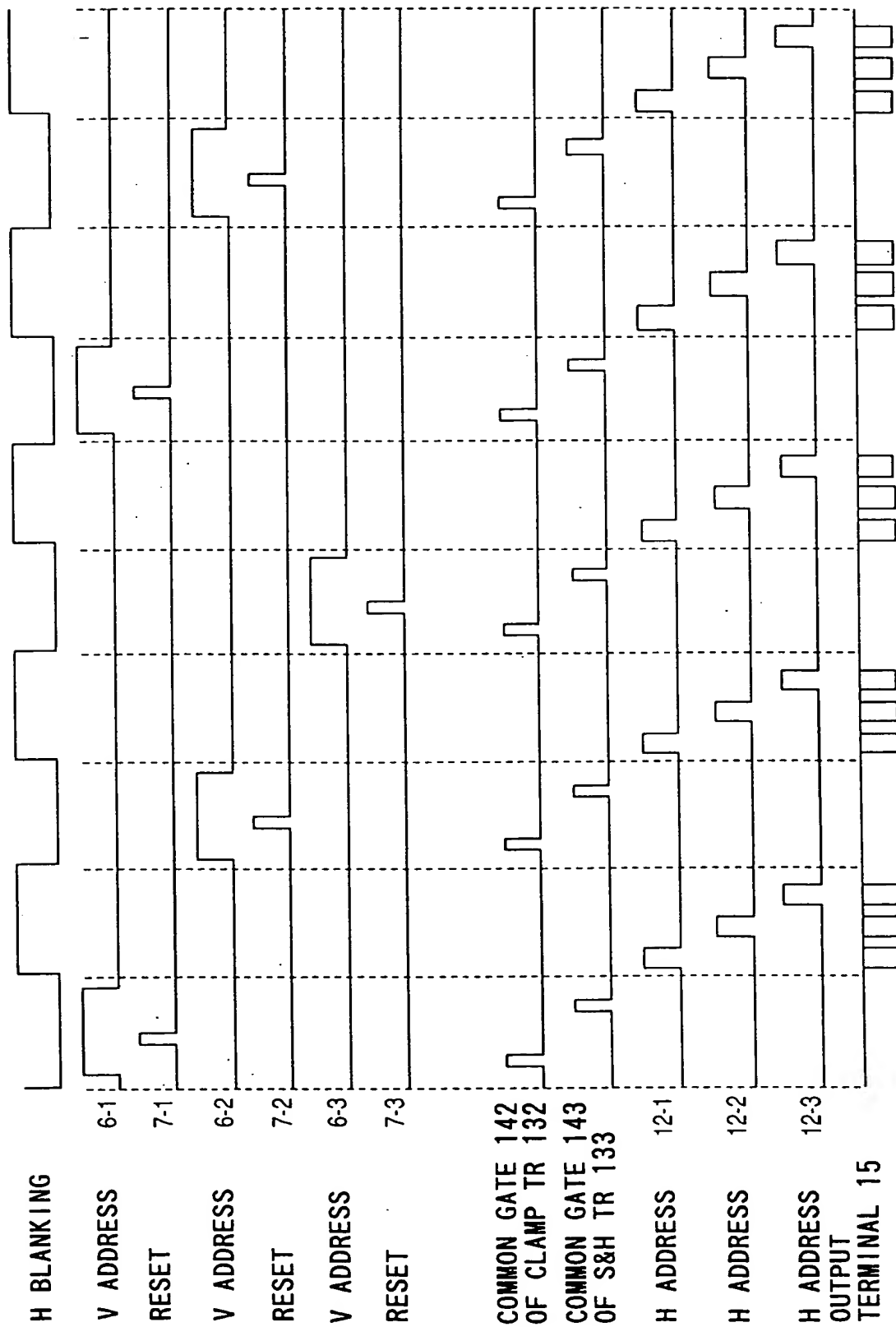


FIG.82

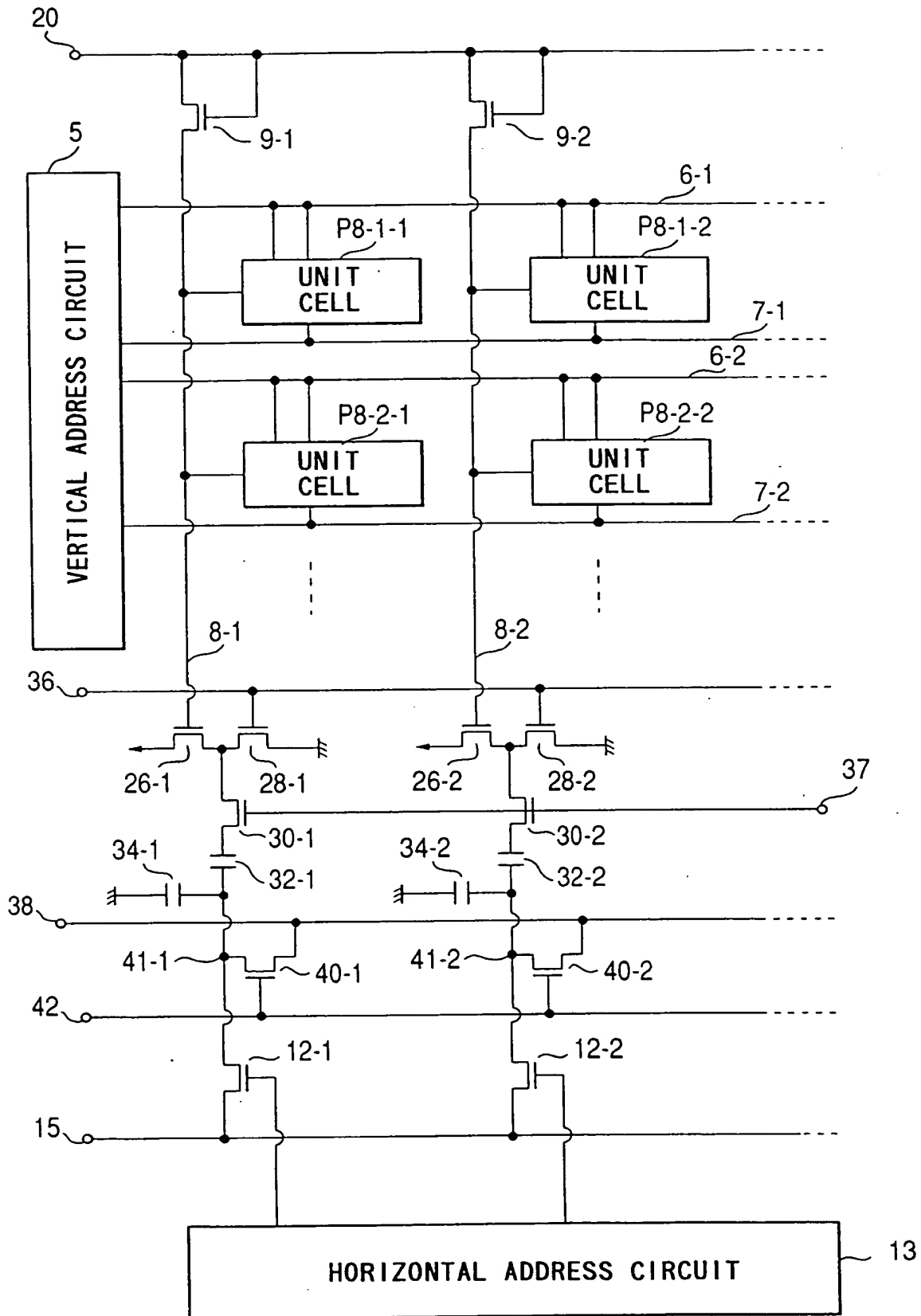


FIG.83

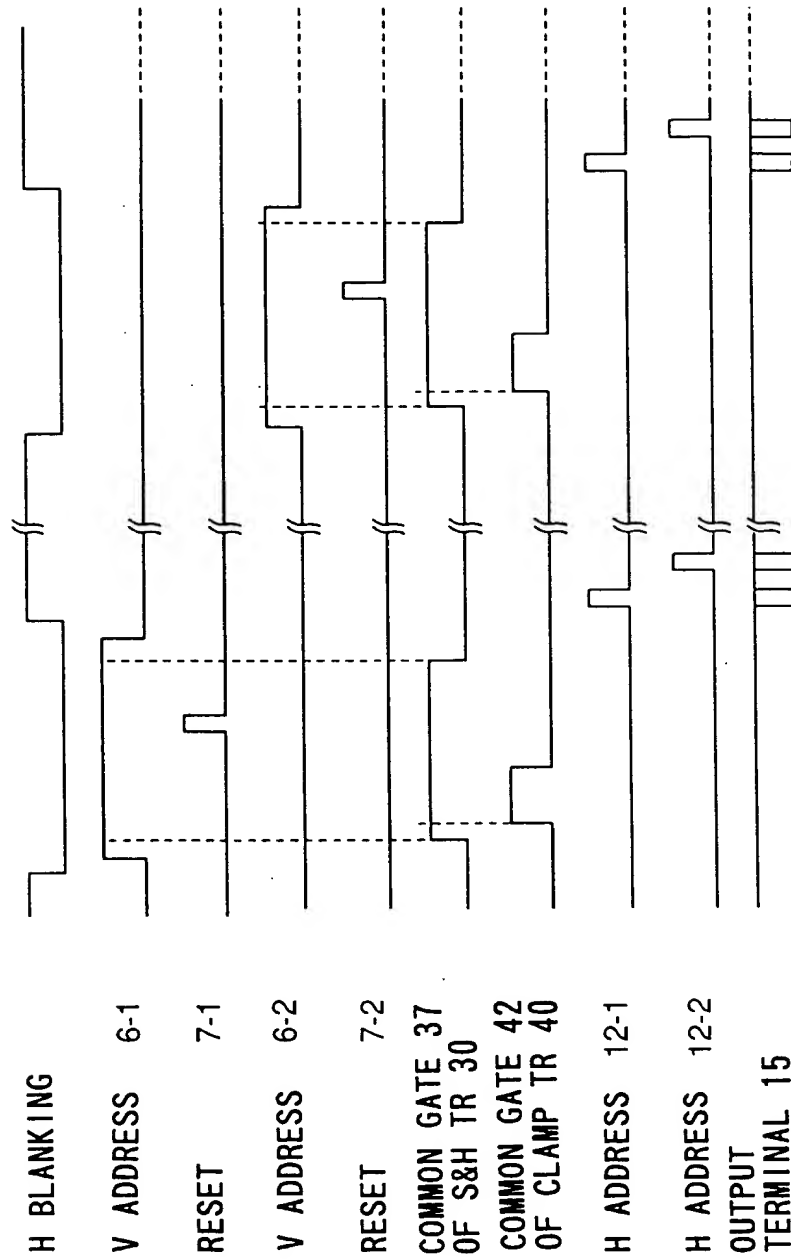


FIG.84



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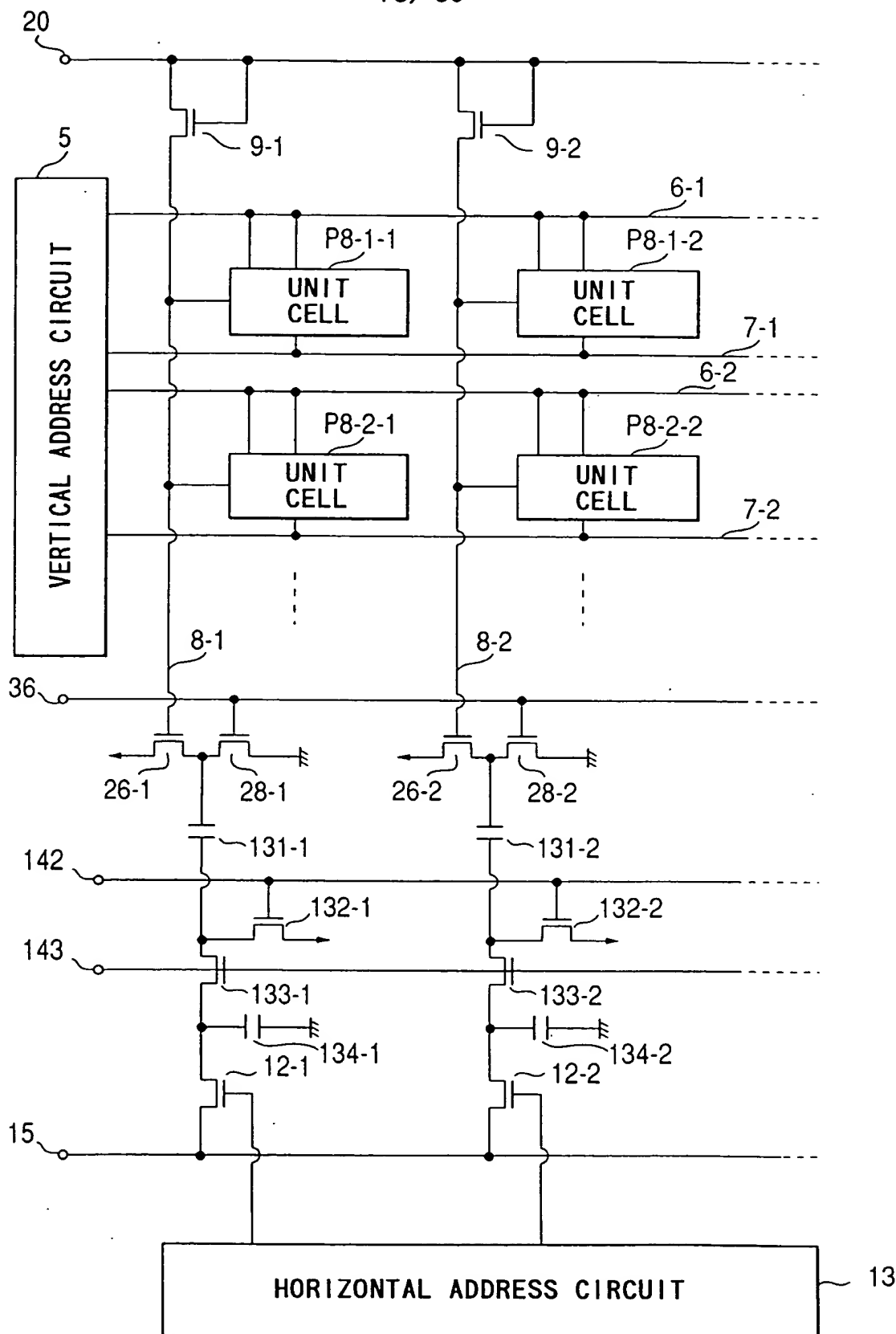


FIG.86

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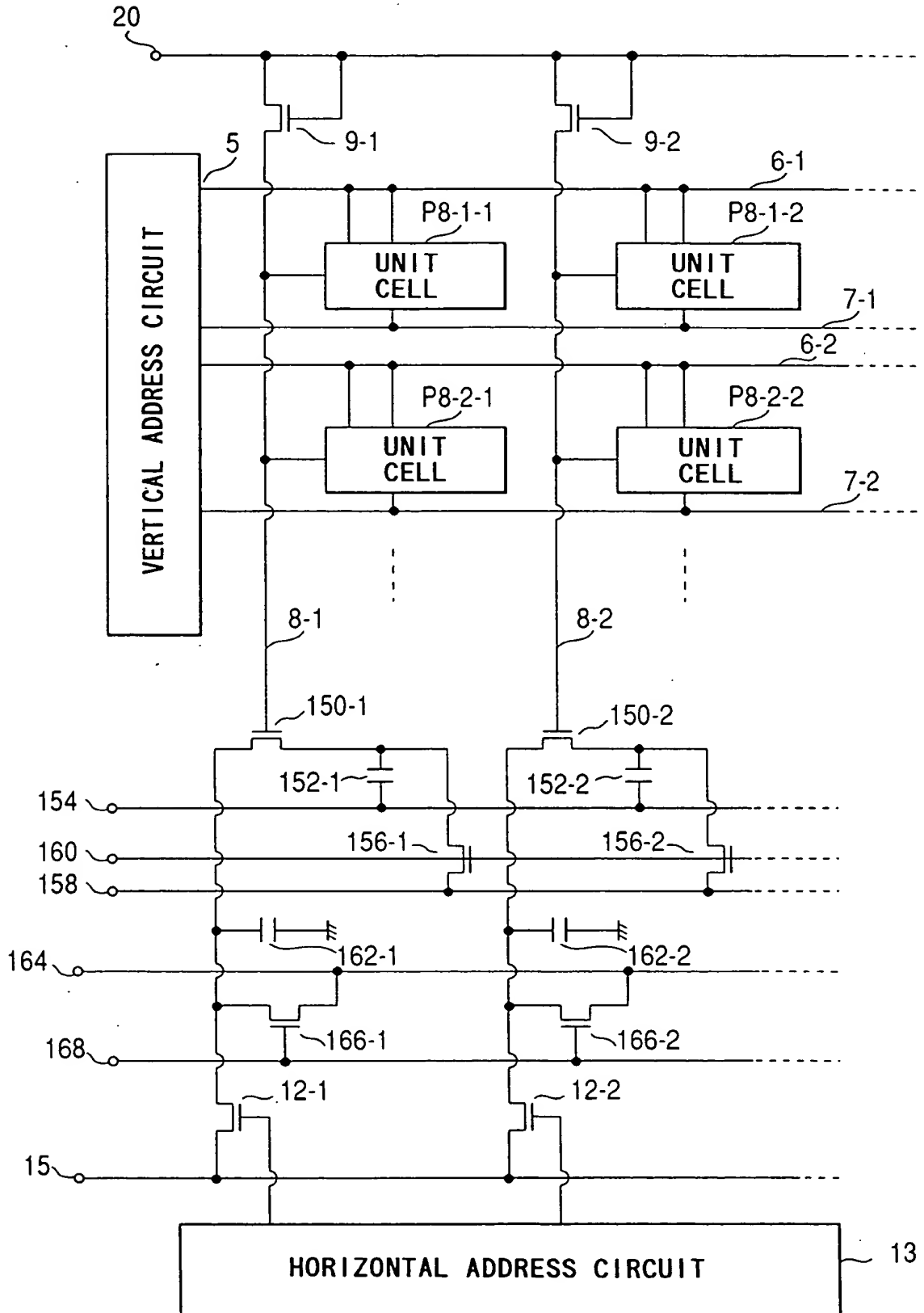


FIG.87

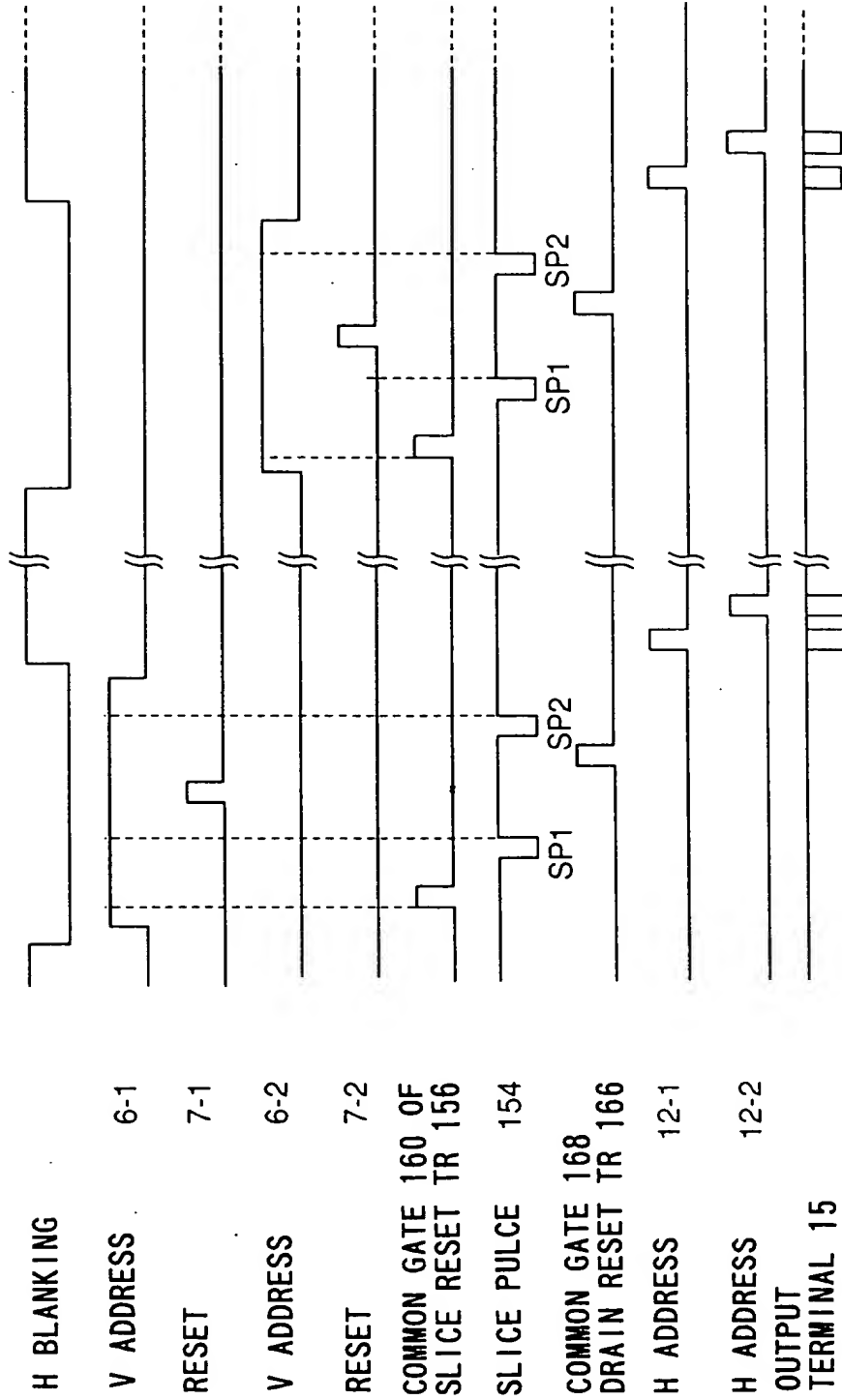


FIG.88

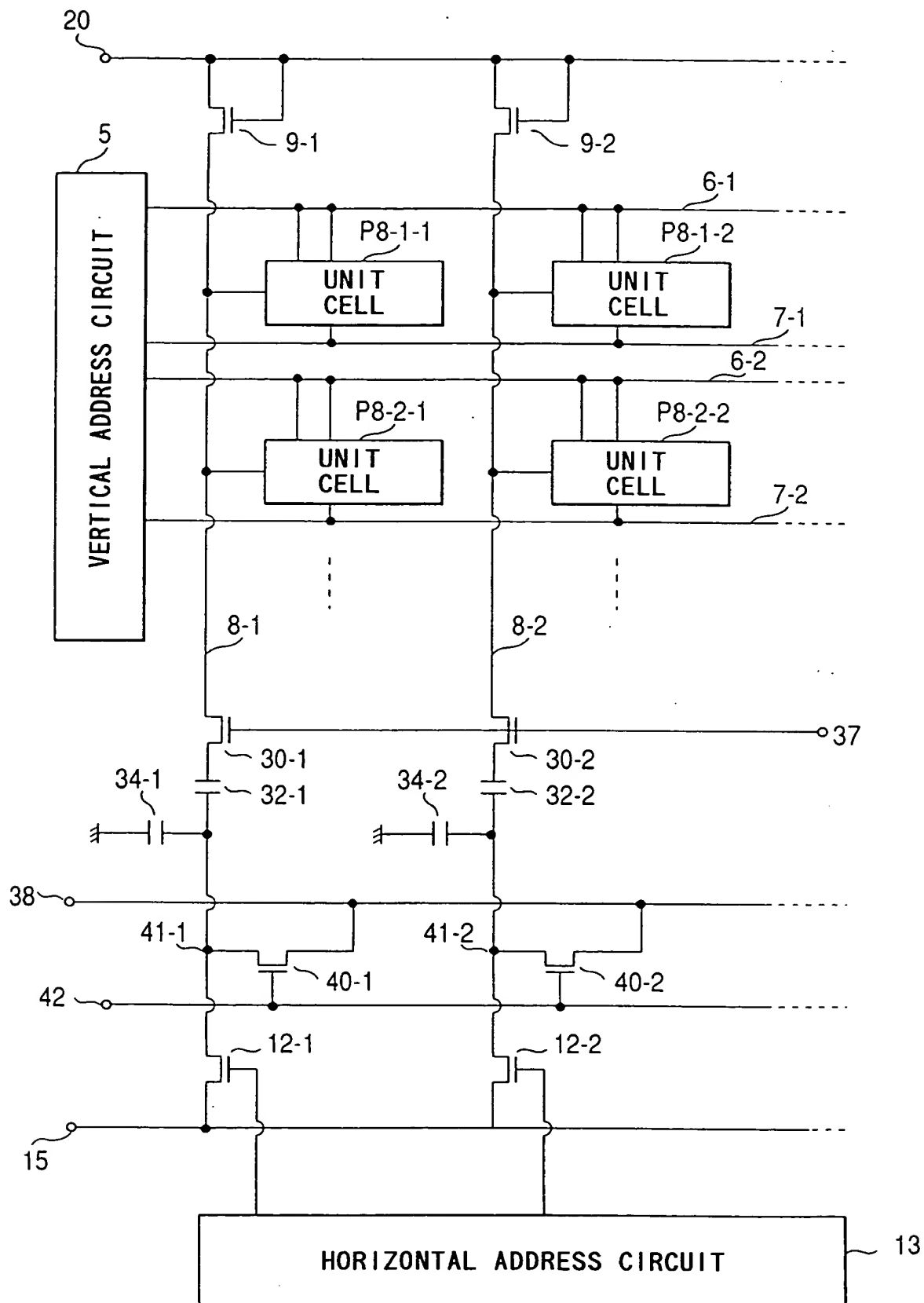


FIG.89

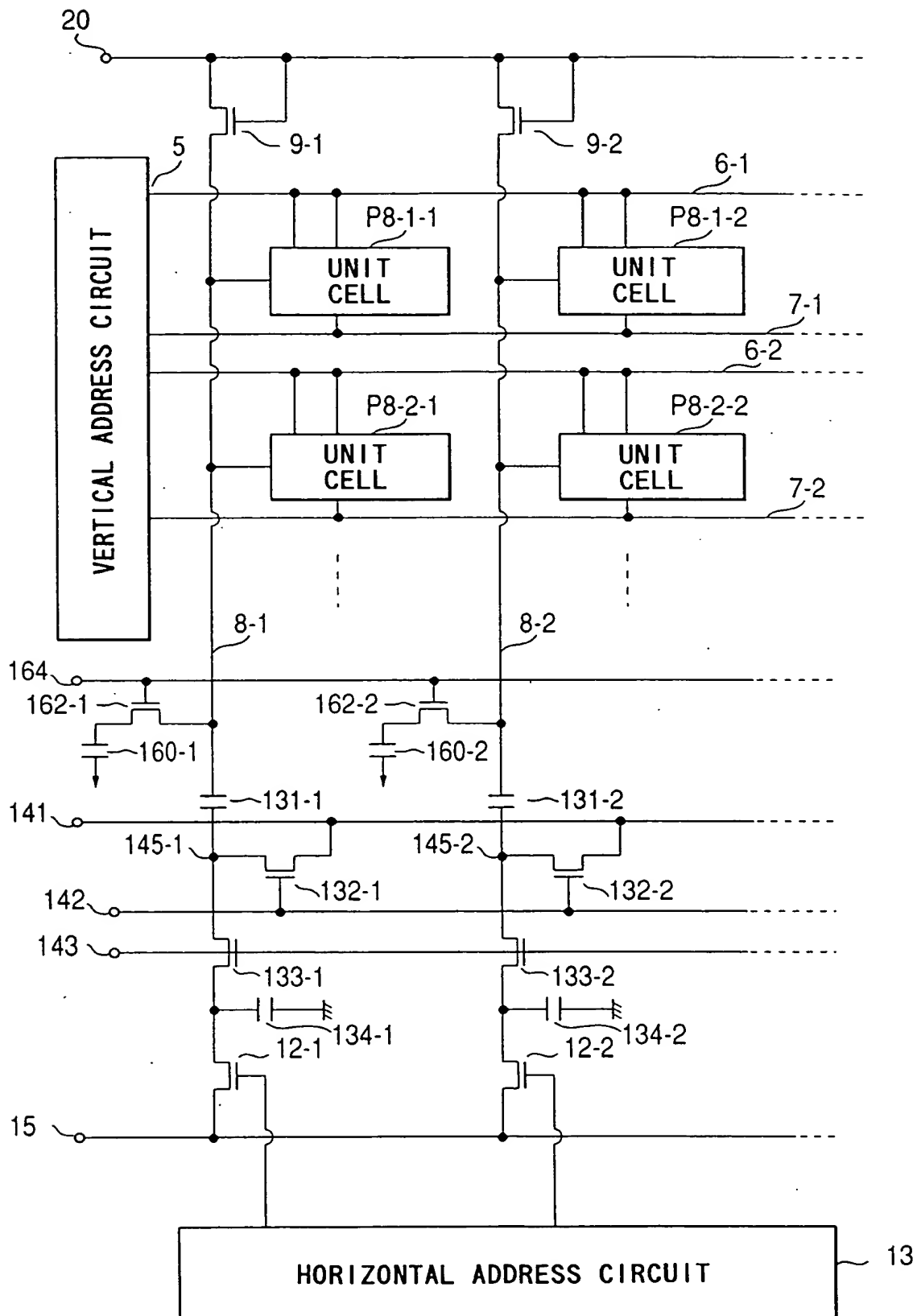


FIG.90

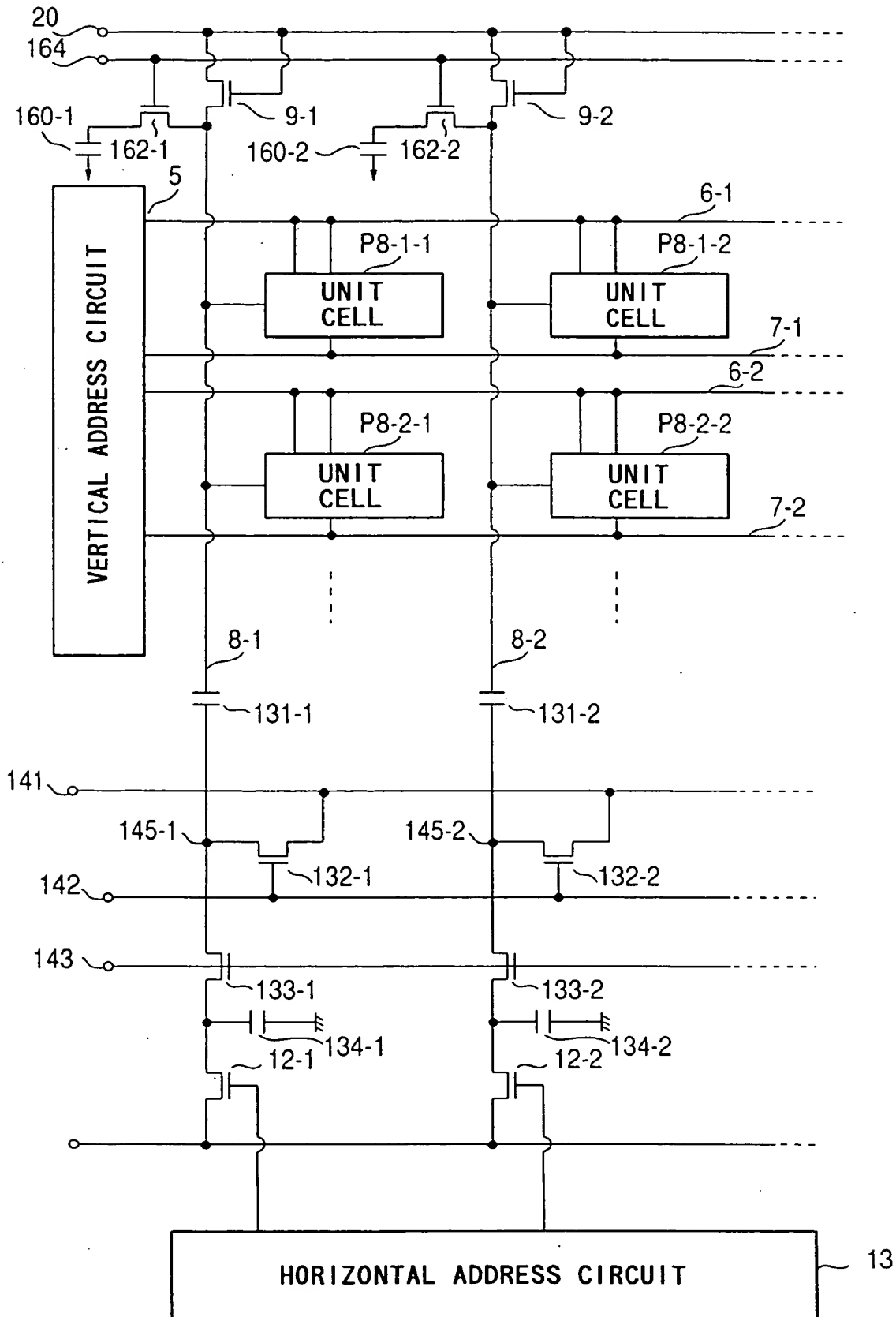


FIG.91

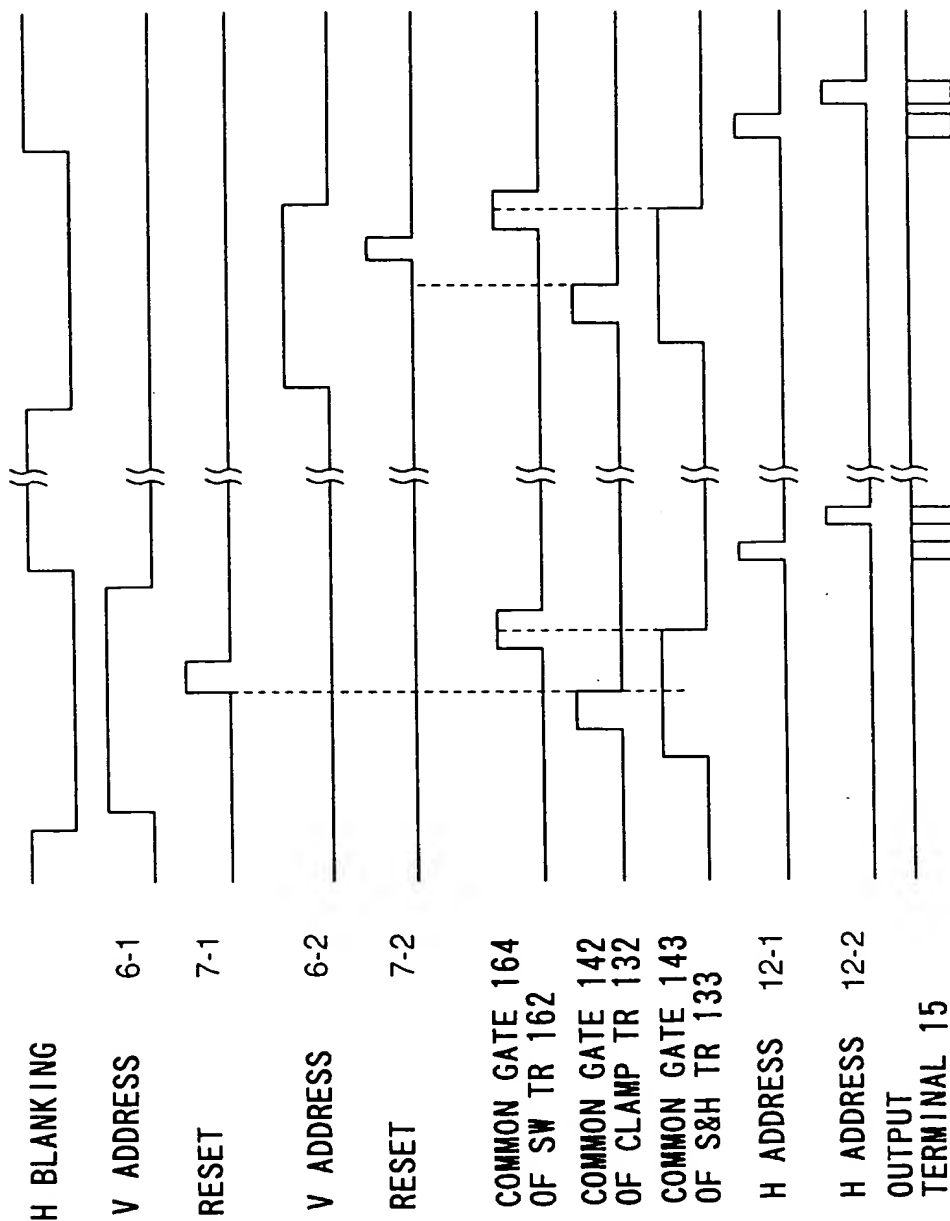


FIG.92

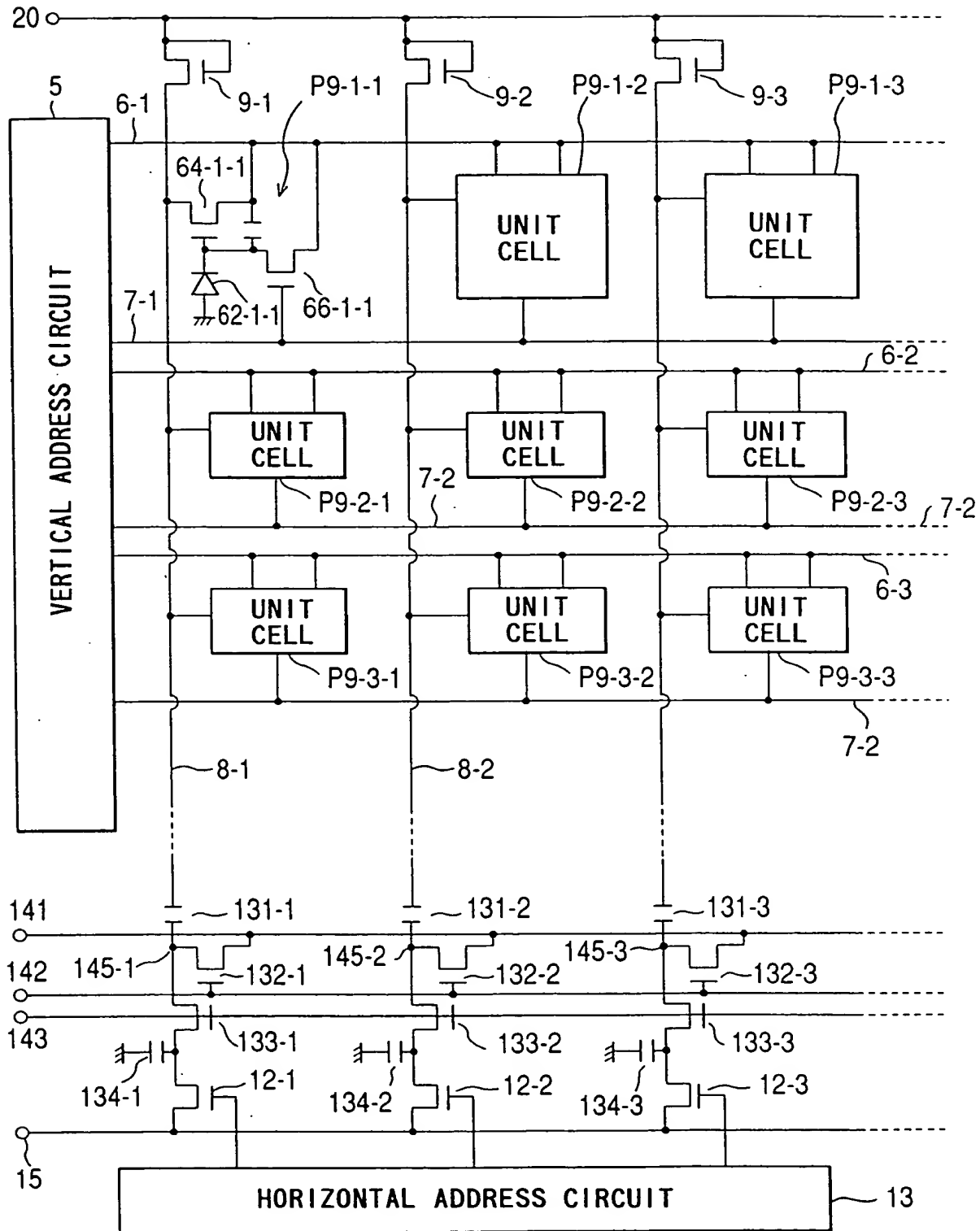


FIG.93

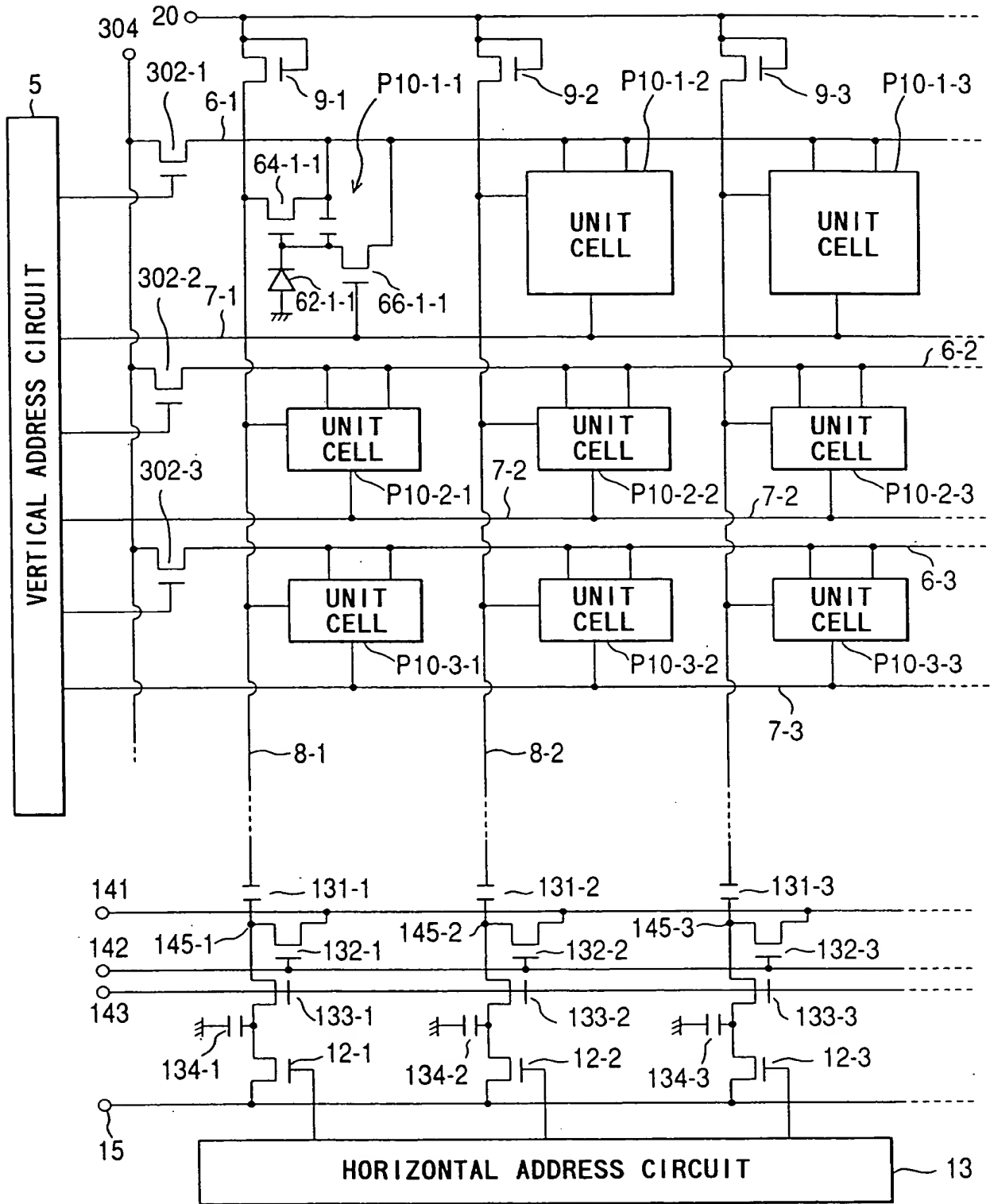


FIG.94

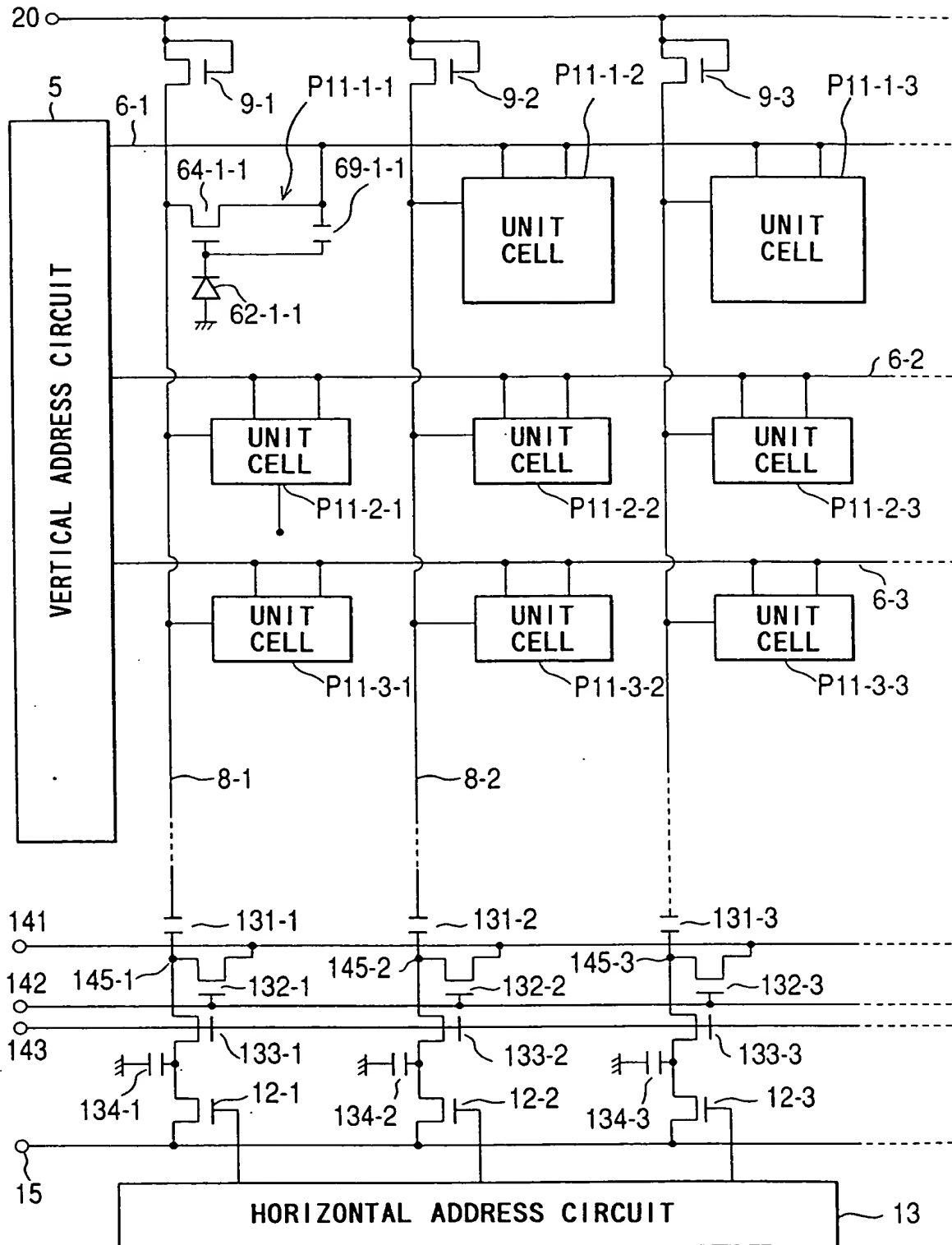


FIG.95

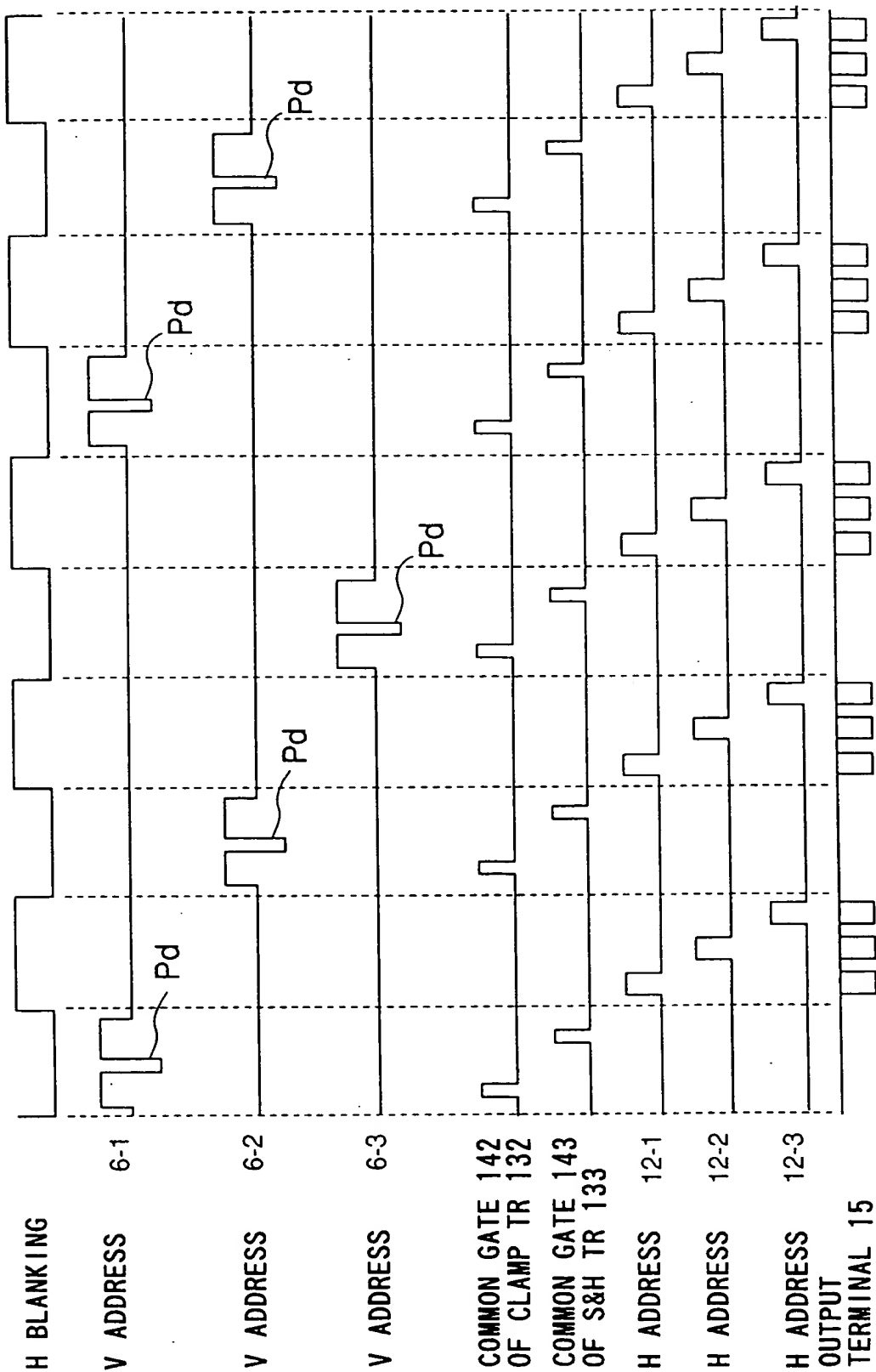


FIG.96

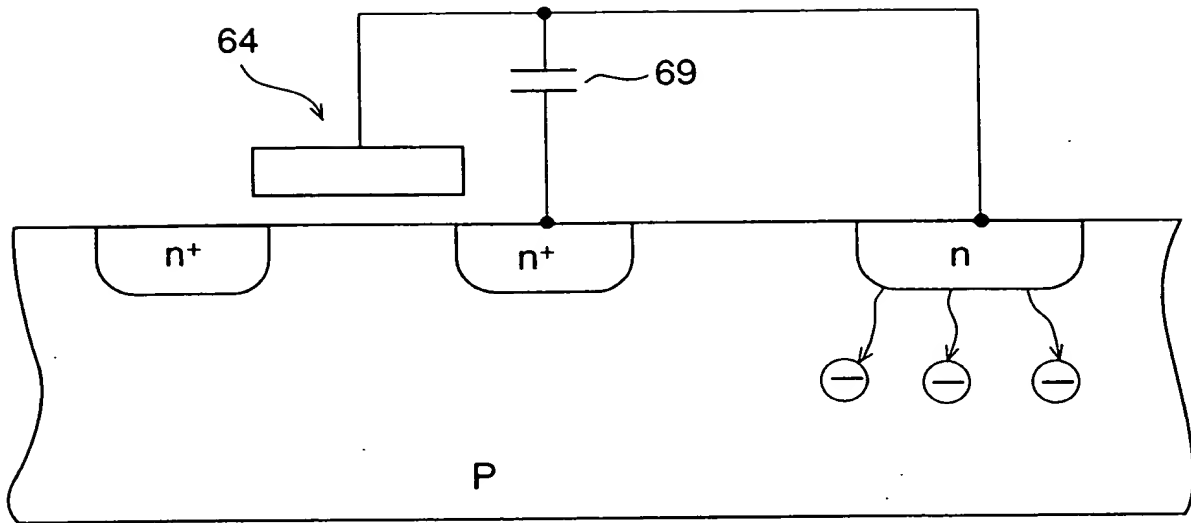


FIG.97

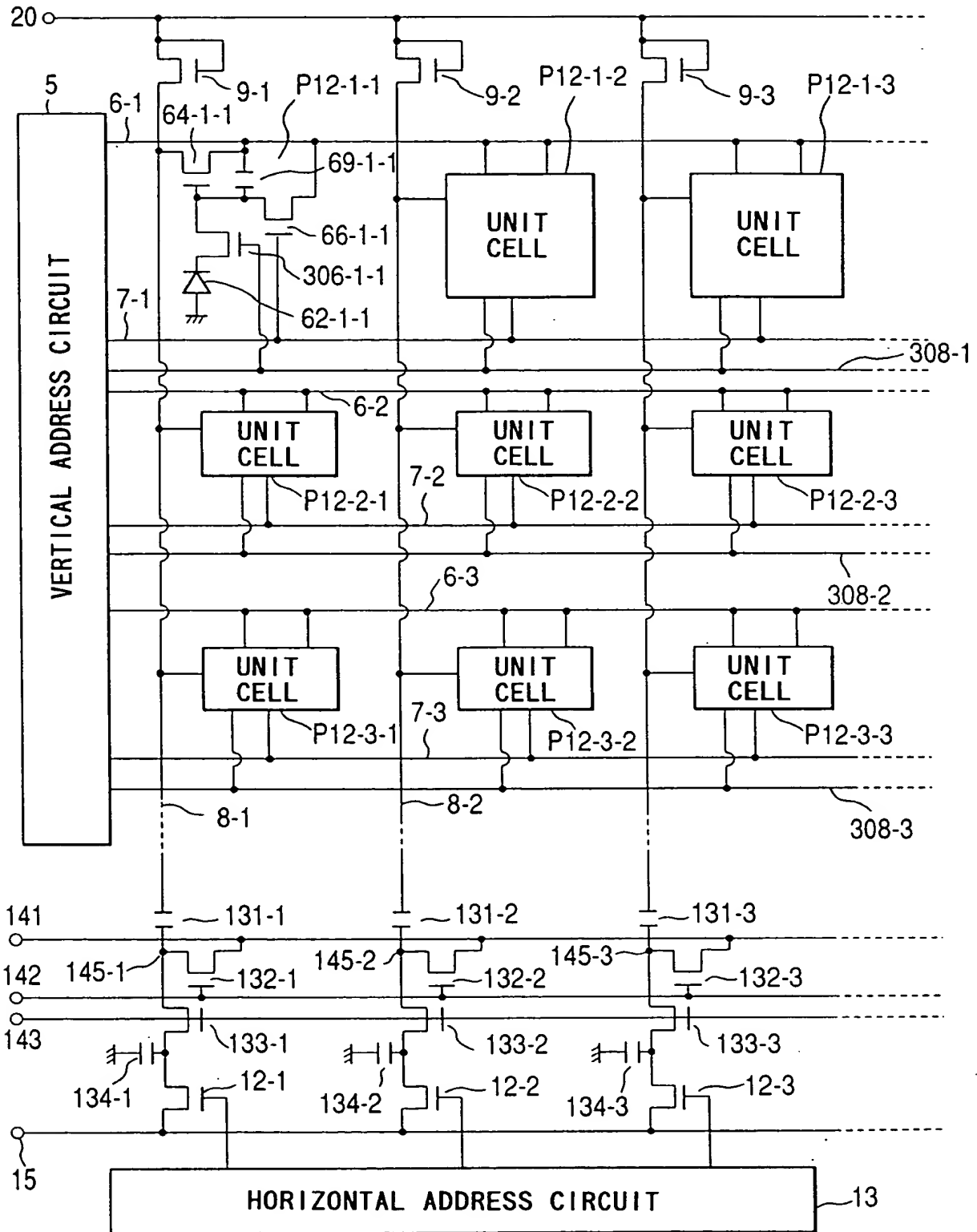


FIG.98



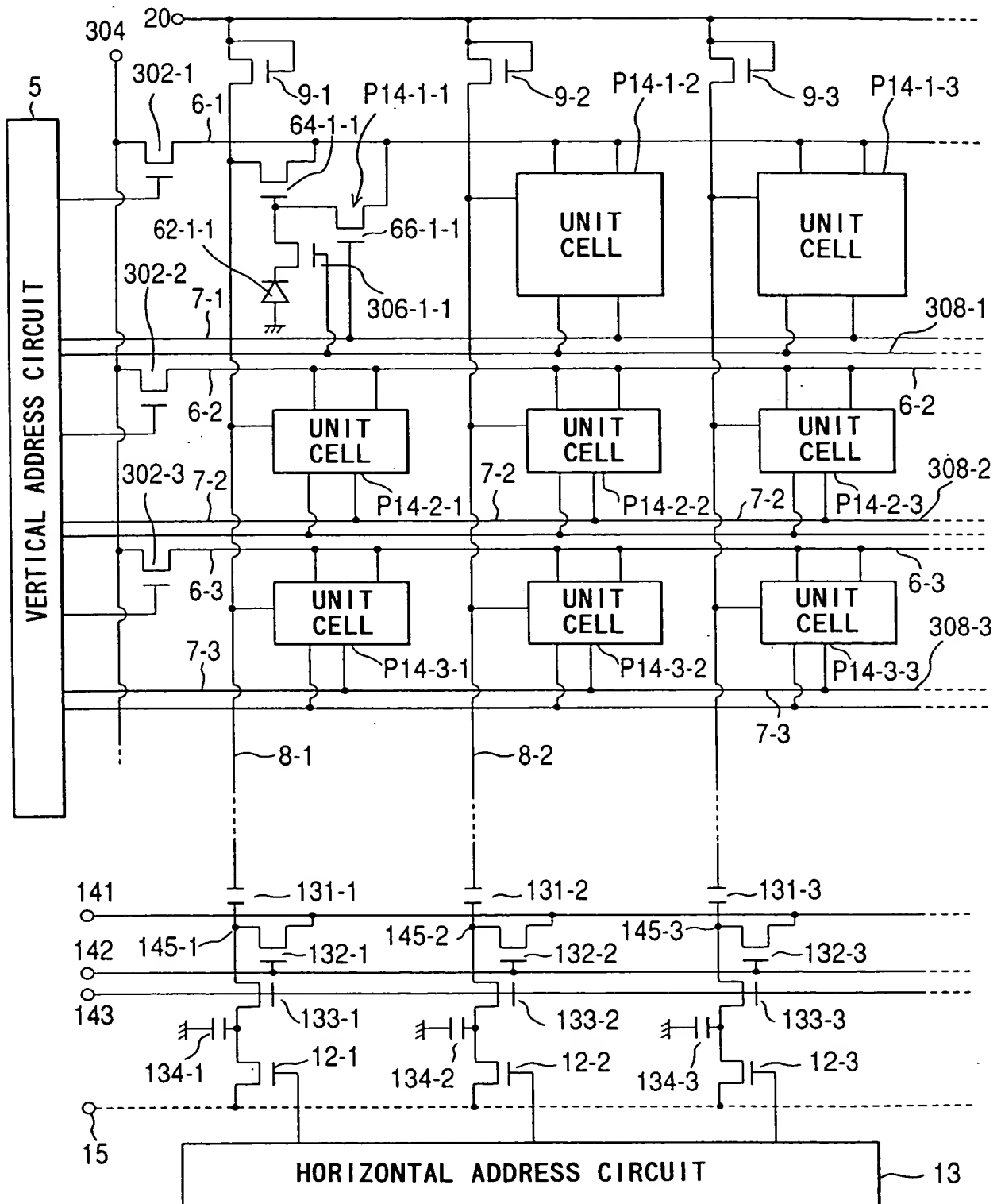


FIG.100

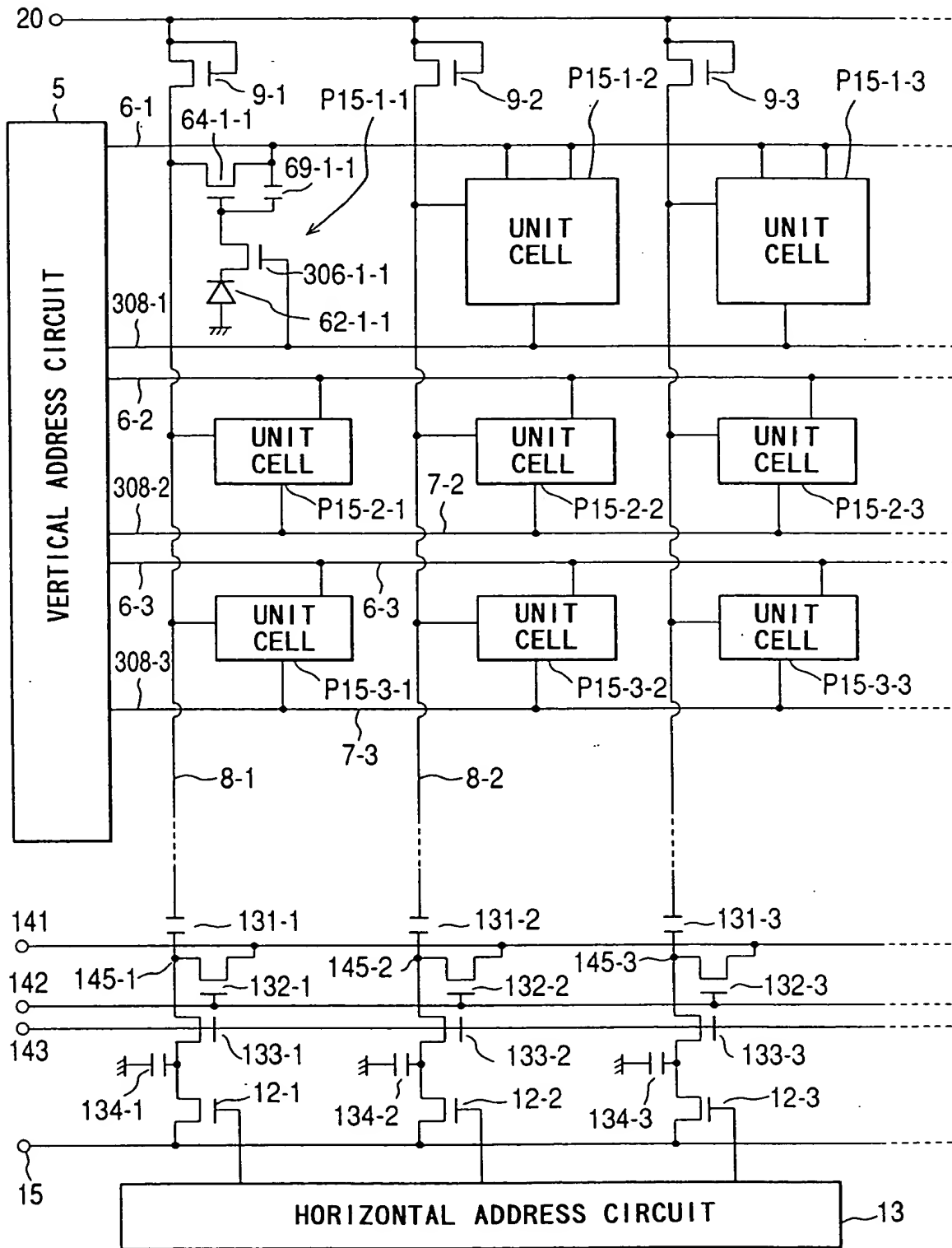


FIG.101

Timing diagram for the 1000 Series Color Receiver. The diagram shows the relationship between various signals over time, with vertical dashed lines indicating specific time points. The signals are labeled as follows:

- H BLANKING
- V ADDRESS 6-1
- CHANGE TRANSFER 308-1
- V ADDRESS 6-2
- CHANGE TRANSFER 308-2
- V ADDRESS 6-3
- CHANGE TRANSFER 308-3
- COMMON GATE 142 OF CLAMP TR 132
- COMMON GATE 144 OF S&H TR 133
- H ADDRESS 12-1
- H ADDRESS 12-2
- H ADDRESS 12-3
- OUTPUT TERMINAL 15

The diagram illustrates the timing of these signals during horizontal and vertical blanking intervals, showing how they are synchronized with the video signal.

FIG. 102

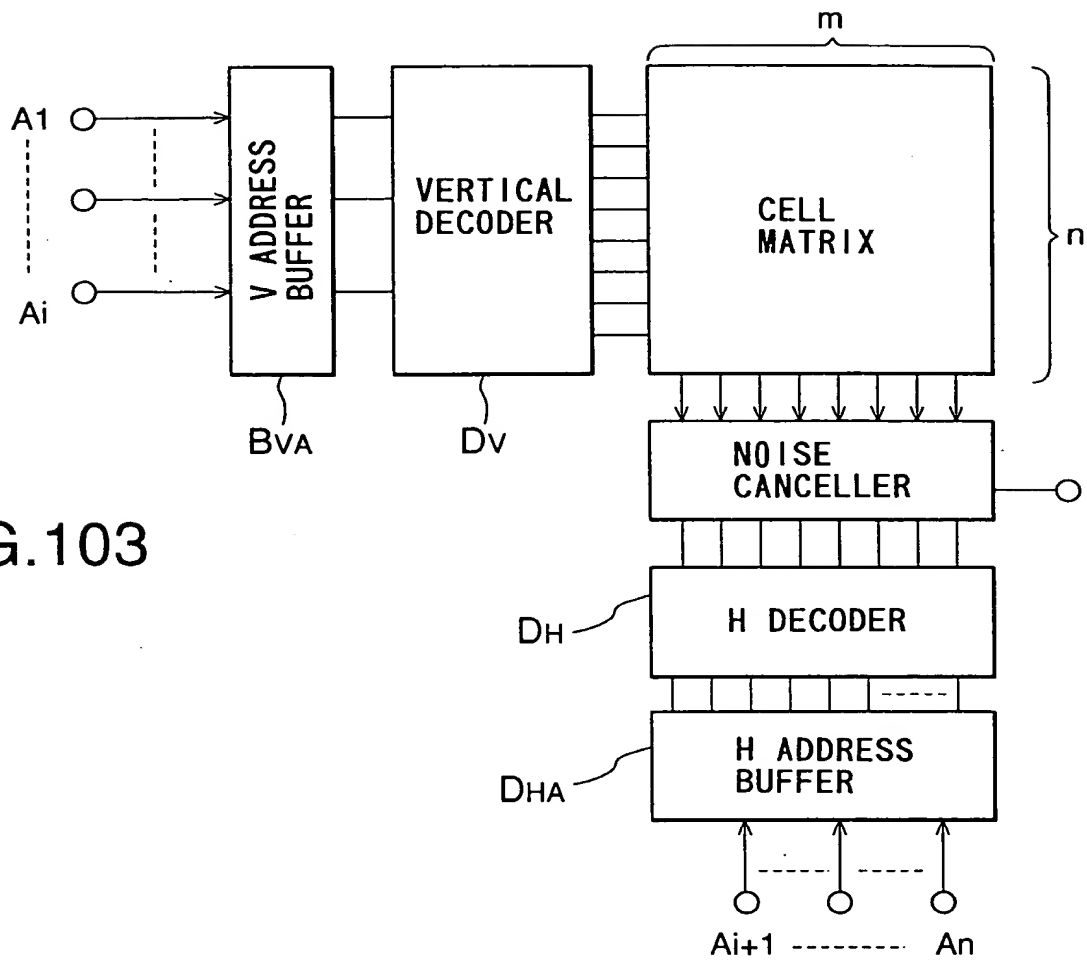


FIG.103

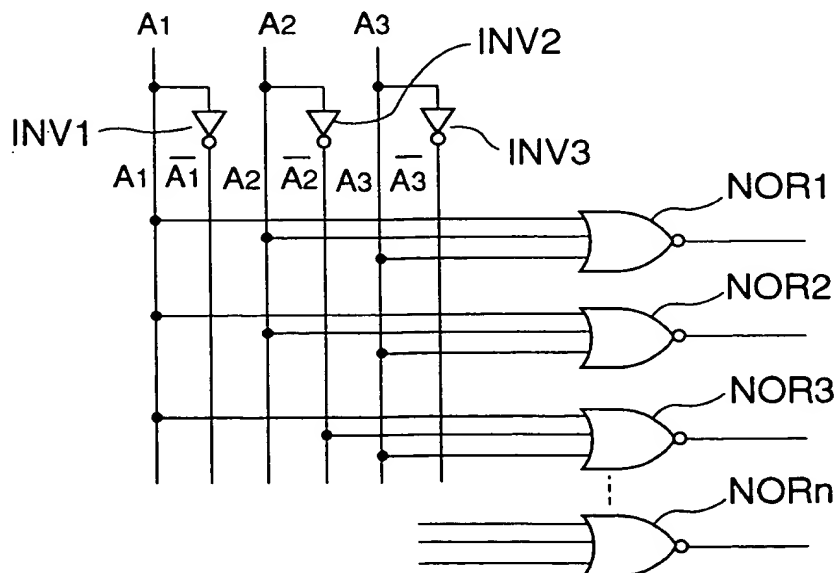


FIG.104